Physical-Layer RF Design of Dual-Band 802.11 WLAN

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Sheng-Fuh Chang, Associate Professor
Center of Telecommunication Research
Department of Electrical Engineering
National Chung Cheng University

(05)2720411-33218, Fax:(05)2720862, ieesfc@ccu.edu.tw

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II. RF Design Requirements from 802.11 PHY Clauses

III. Design Example: Dual-Band WLAN RF Module

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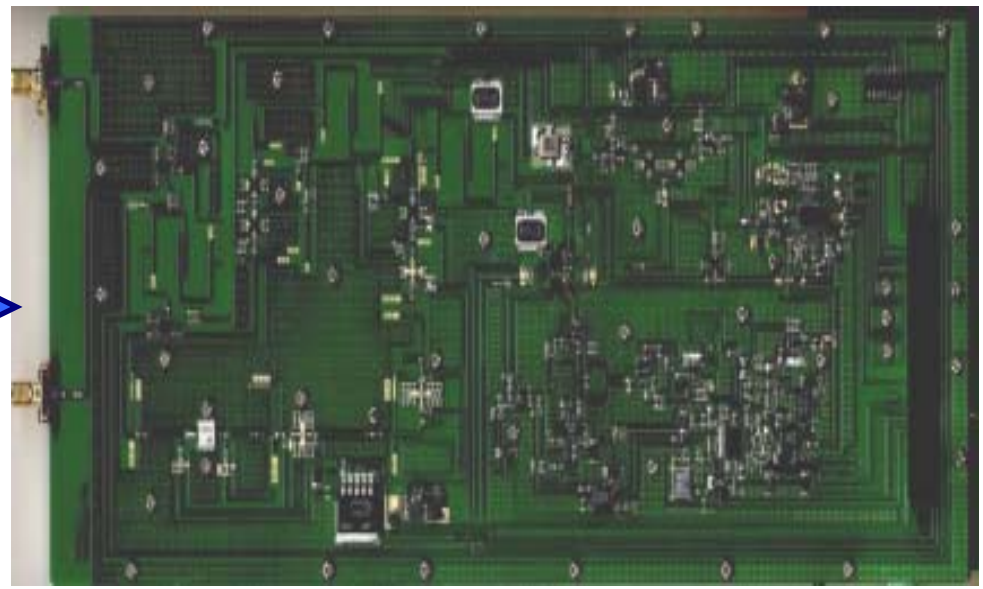
I. Motivation of the Research

How do we turn *802.11 WLAN RF written document* into a *physical module*?



II. RF Requirements from 802.11 PHY Clauses

- *IEEE802.11a*-Subclause 17.3

  OFDM PLCP(Physical Layer Convergence Procedure) Sublayer

- *IEEE802.11b*-Subclause 18.4

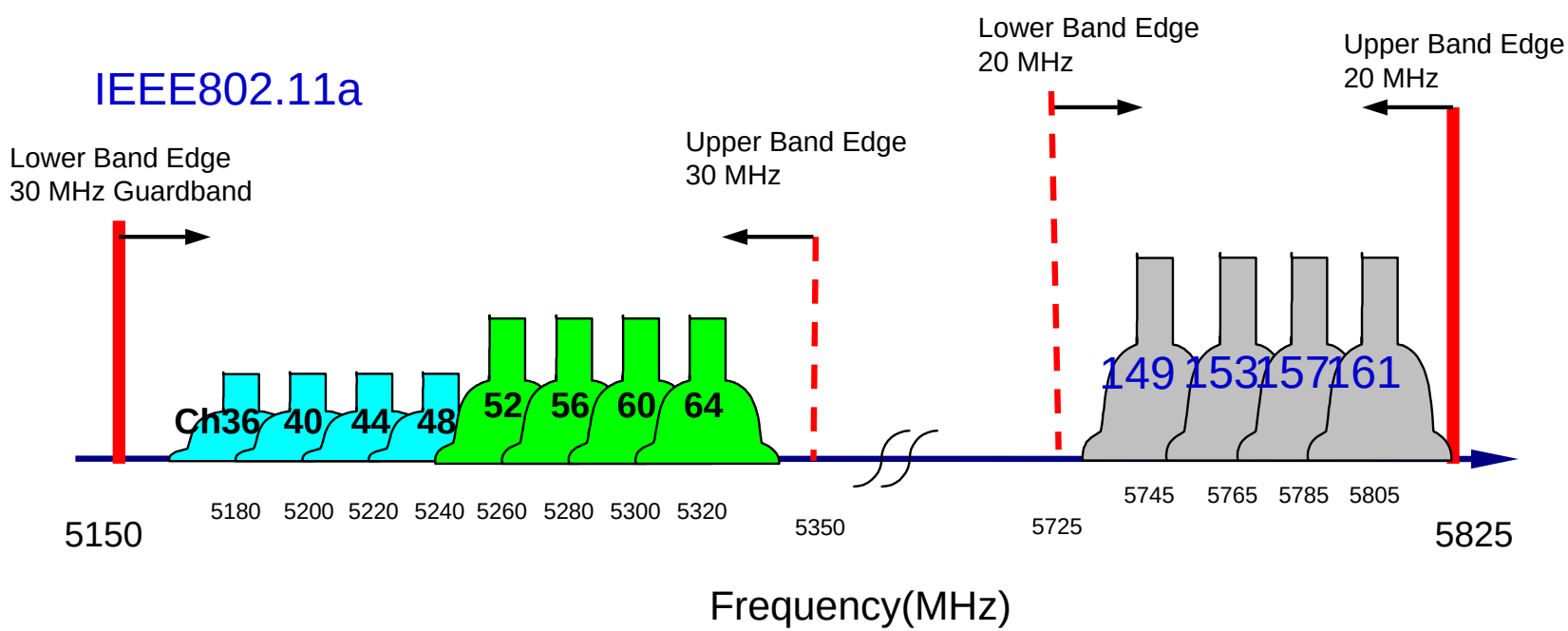
  High Rate PMD(physical medium dependent) Sublayer

- *IEEE802.11g*-Subclause 19.4

(I) Operation Frequency Band and channel number

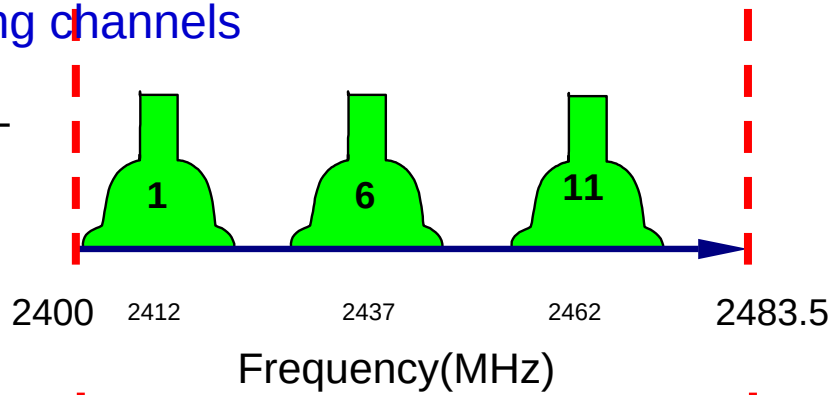
IEEE802.11a 17.3.8.3

Channel Center Frequency=5000 + 5n_{ch} (MHz), where n_{ch}=0,1,…,200

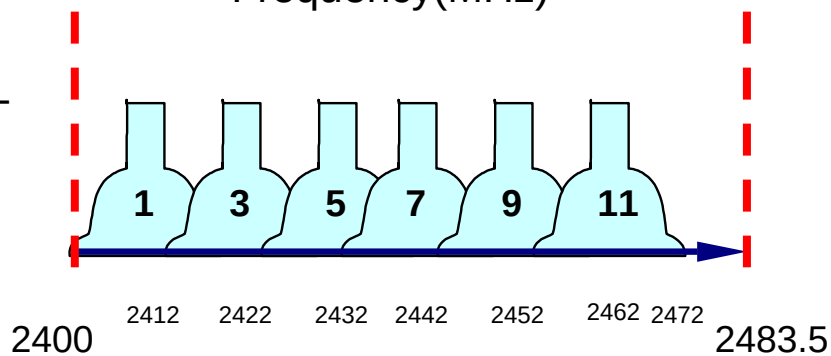


IEEE802.11b/g 18.4.6.7.2 Operating channels

- North American channel selection—non-overlapping

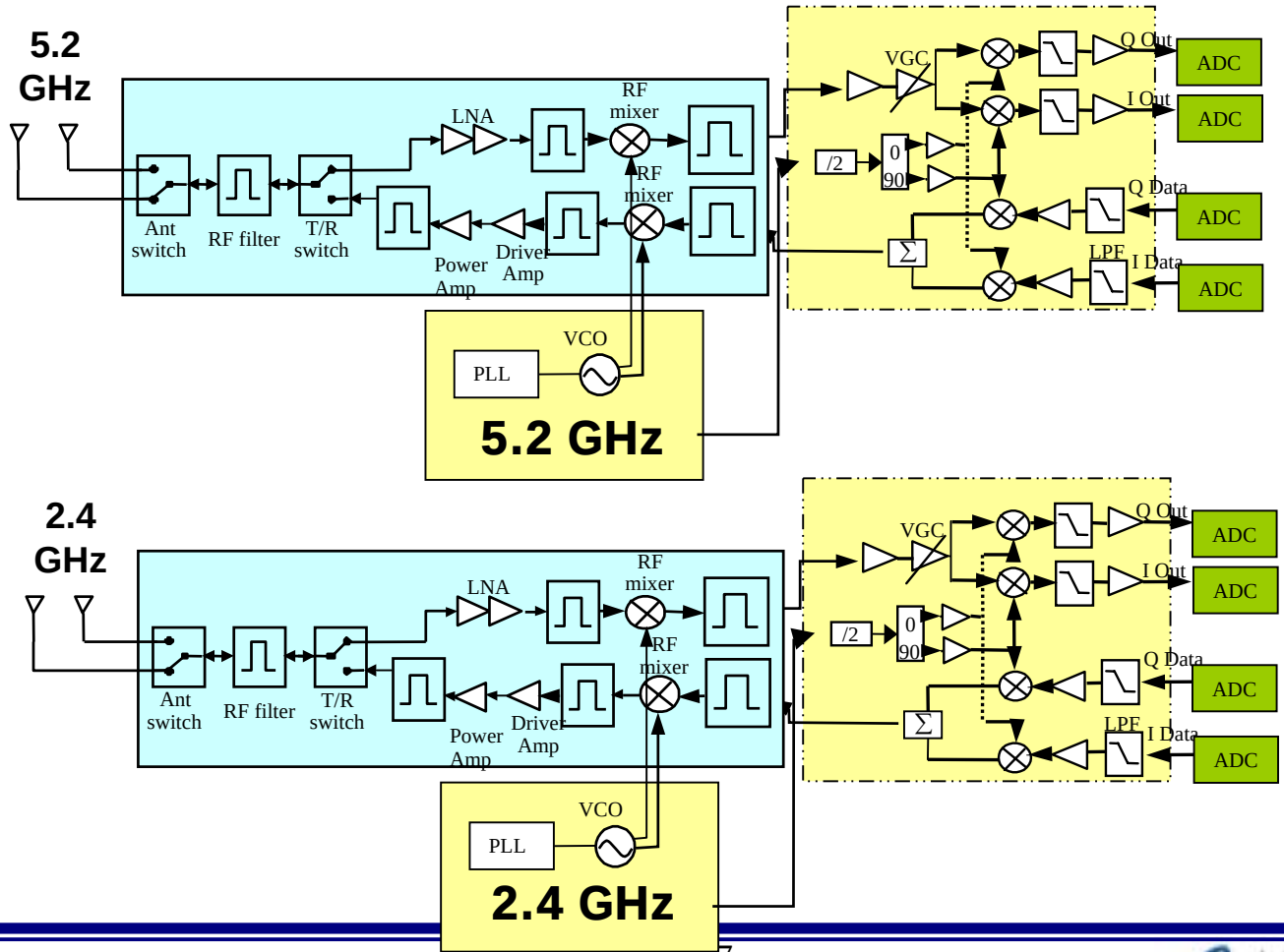


- North American channel selection—overlapping

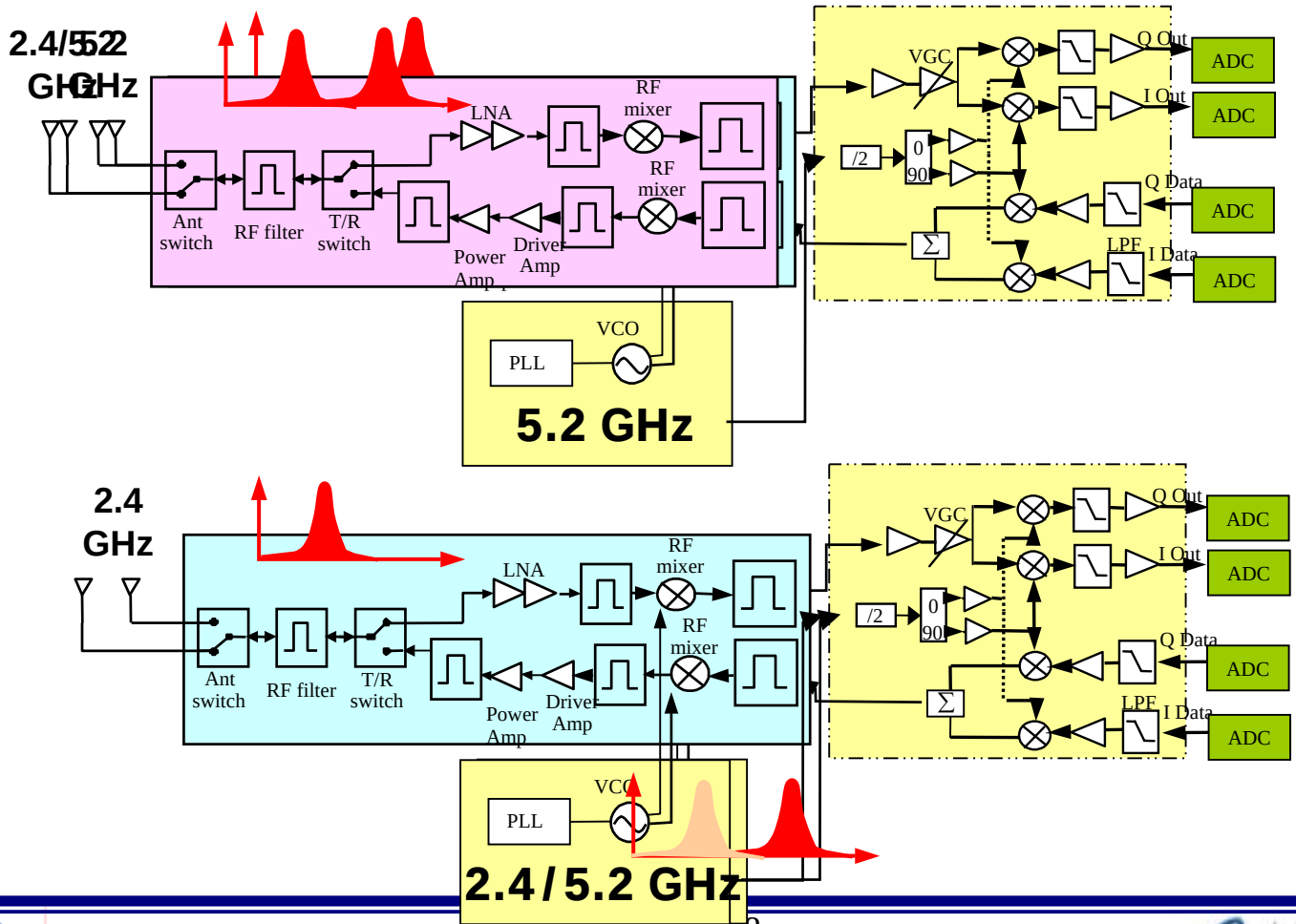


Related to Transceiver architecture, VCO and Frequency Synthesizer Design

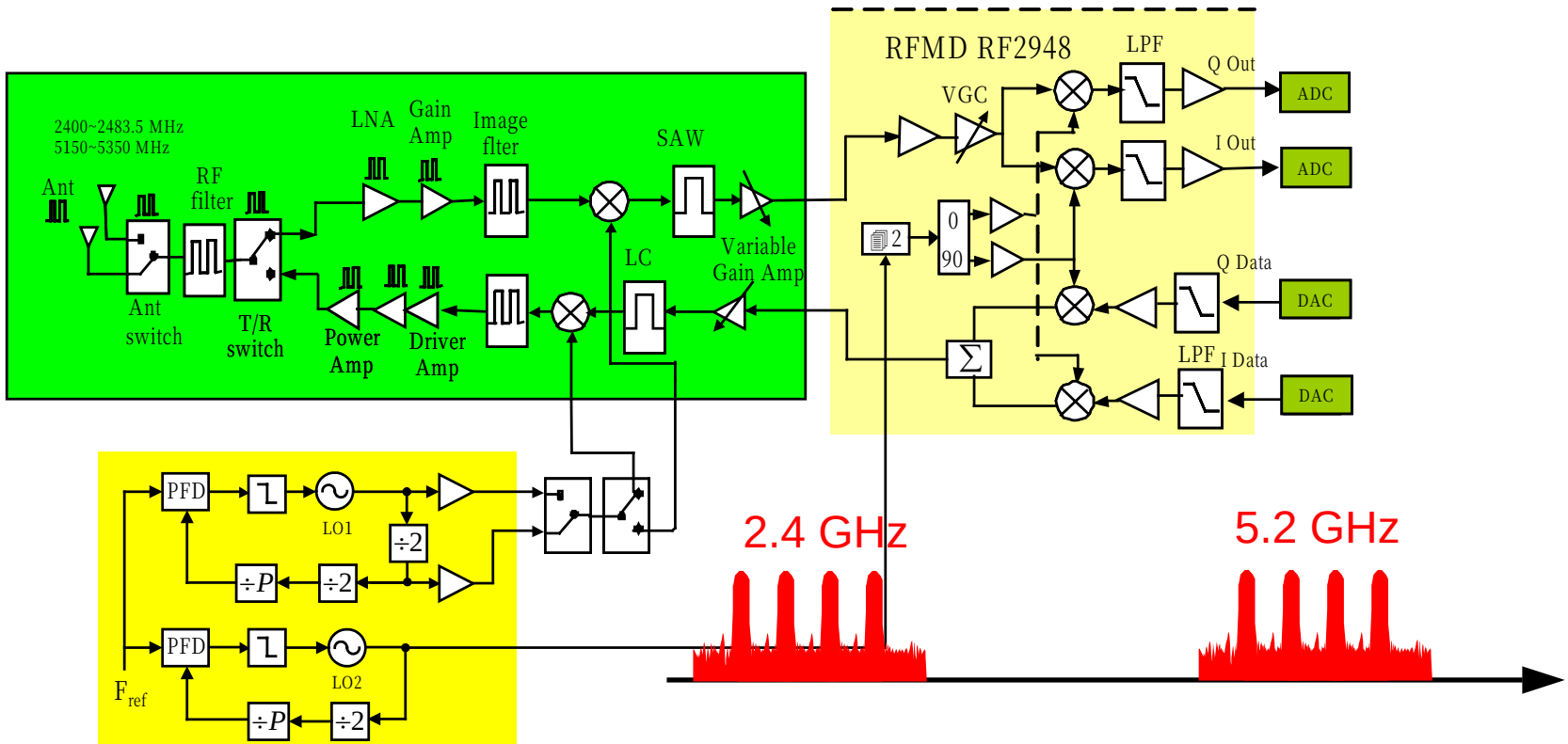
Straight-forward architecture: Two separated RF Transceiver



Cost-Effective architecture: Dualband RF Transceiver

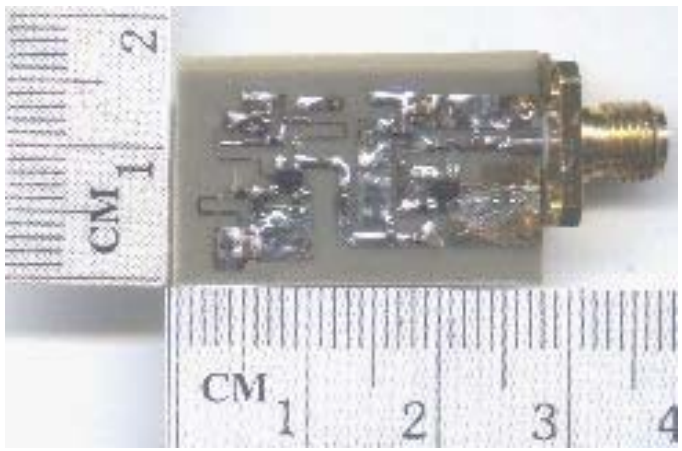


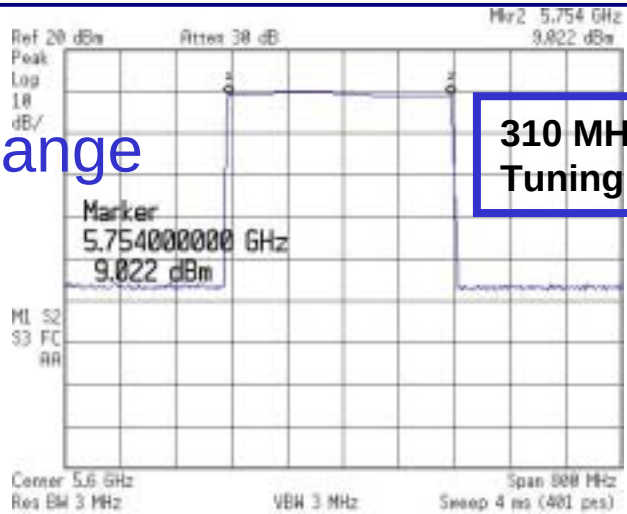
single PLL and VCO generates all RF channels in 2.4 and 5.2 GHz Band



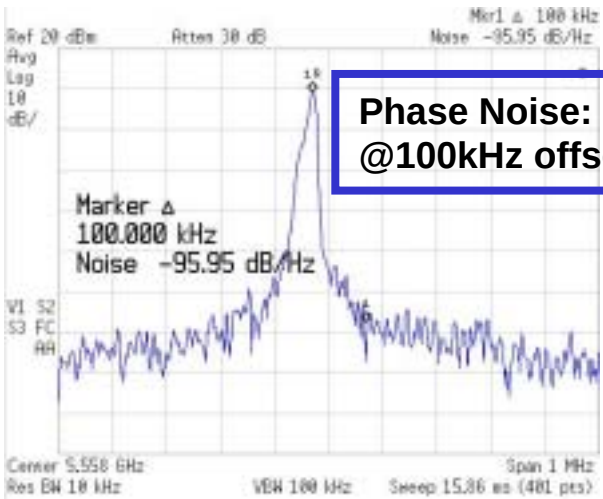
VCO must have

- adequate frequency tuning range
- Low phase noise



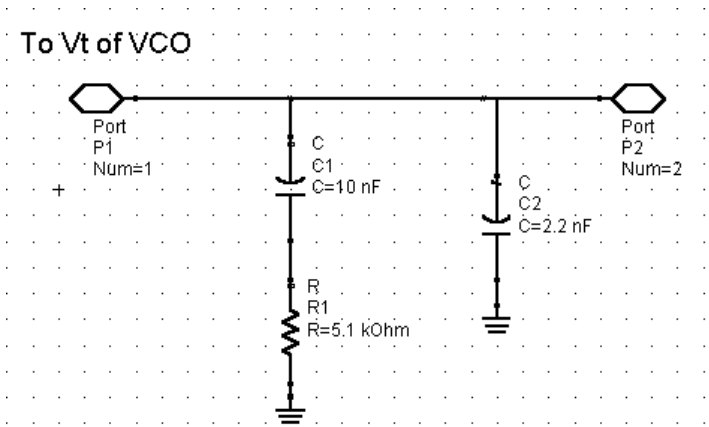


310 MHz Tuning Range



Phase Noise: -96 dBc/Hz @100kHz offset

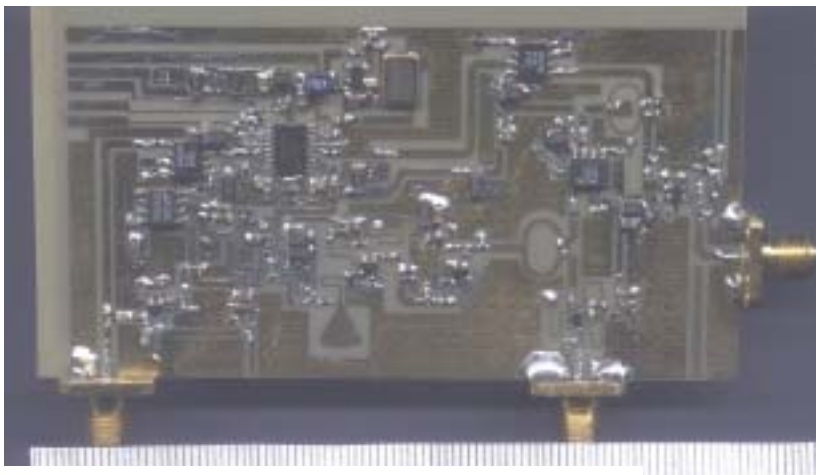
PLL Loop filter design

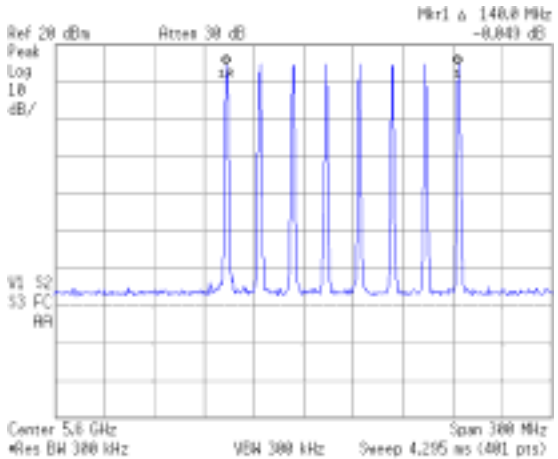


Loop filter is designed with compromise among

- stability (phase margin),
- carrier frequency settling time (Lock time), and
- phase noise and interfering spurs.

Dual-Band Frequency Synthesizer

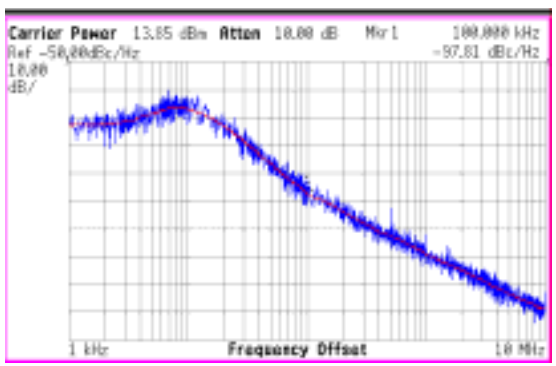


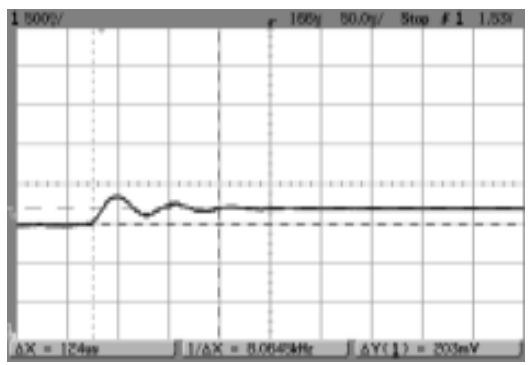


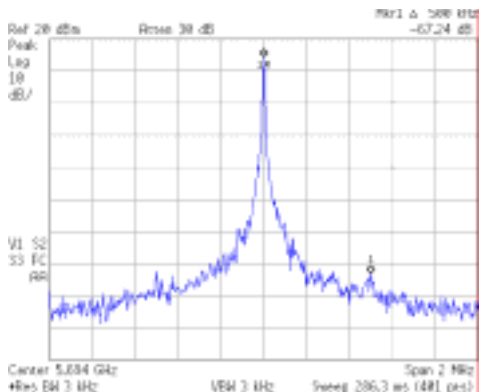
-97.8 dBc/Hz phase noise at 100 kHz off 5693 MHz

124 μS settling time

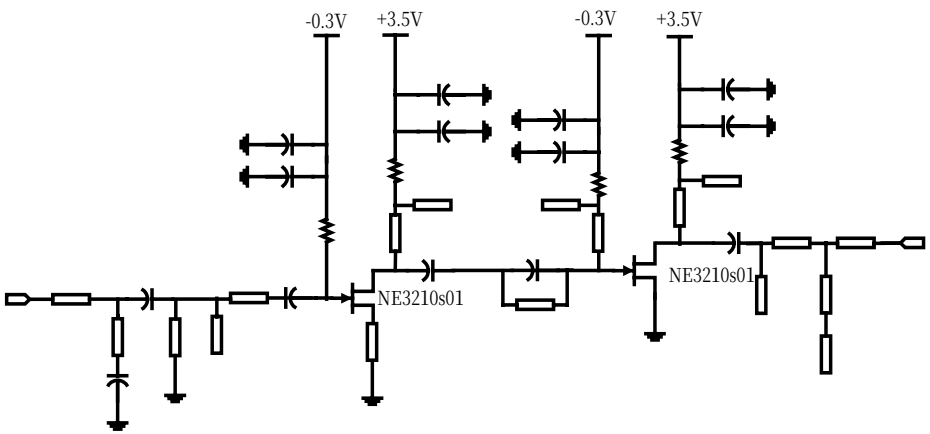
-67 dB spur level

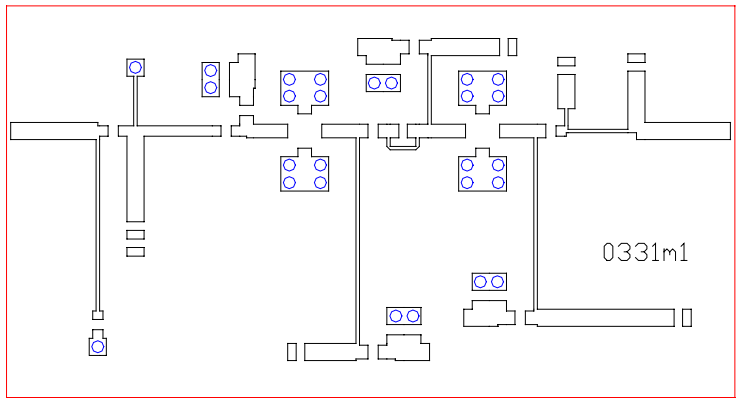


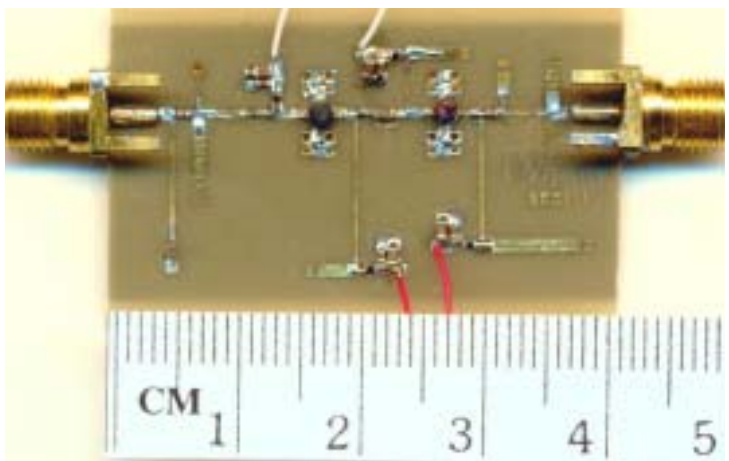


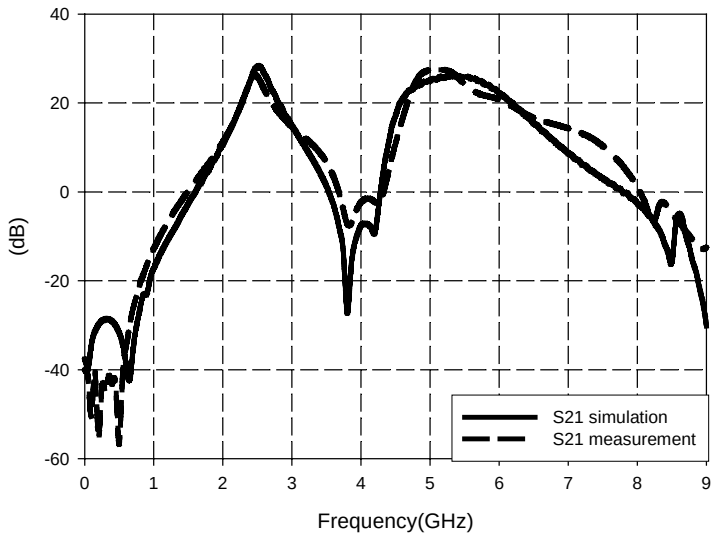


(1) Concurrent Dual-Band LNA- Circuit 1

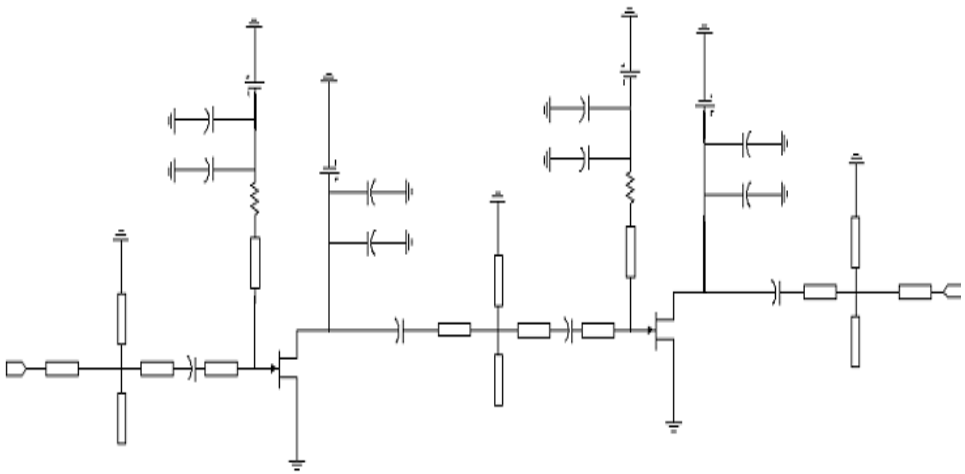


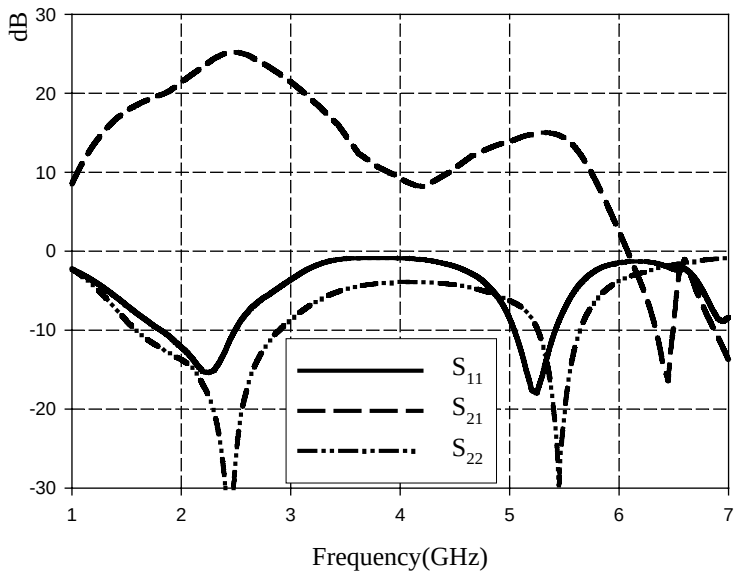


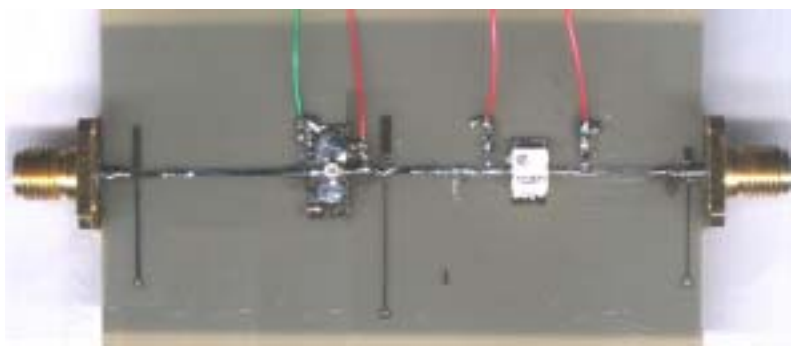




(2) Dual-Band PA

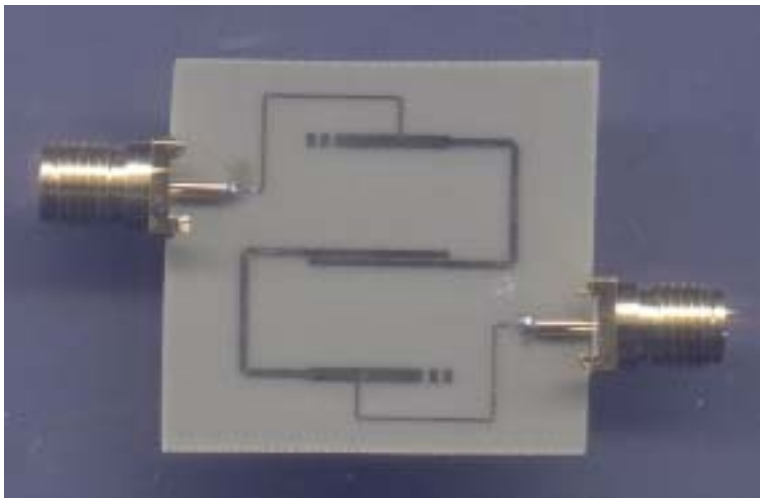


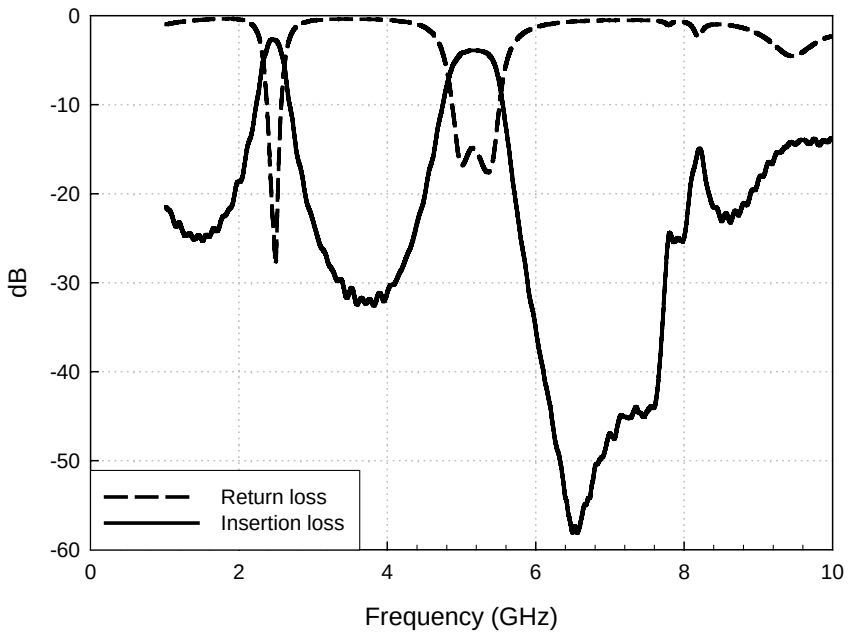




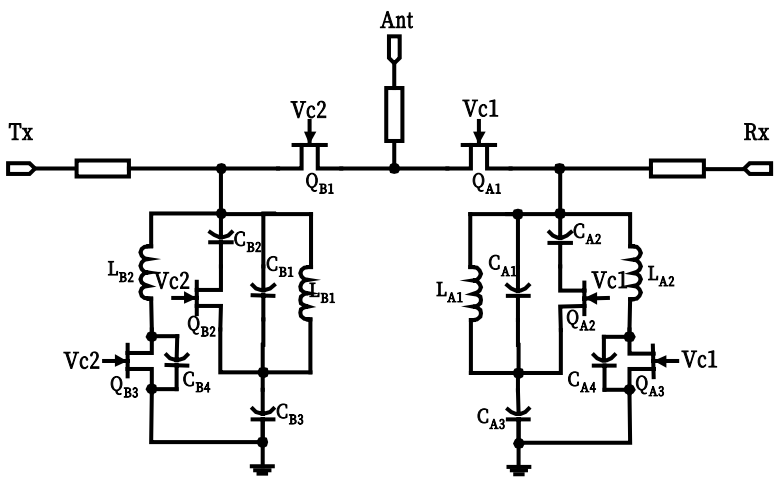
(3) Dual-Band Filter

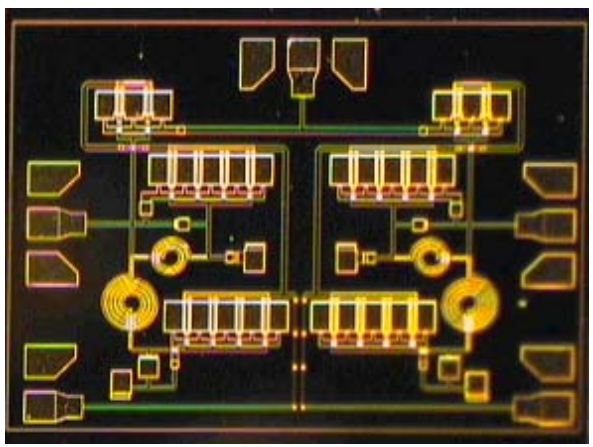
Second-order SIR filter

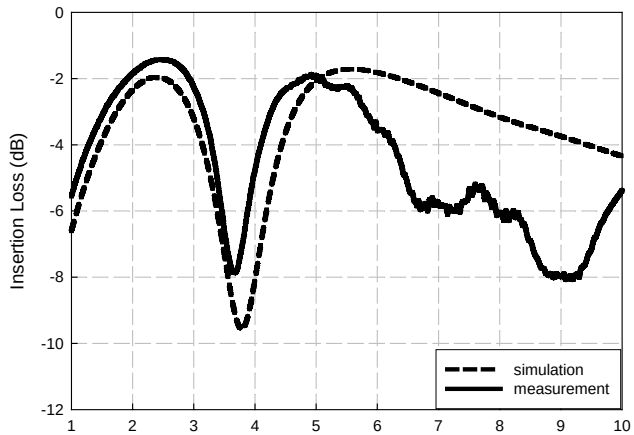


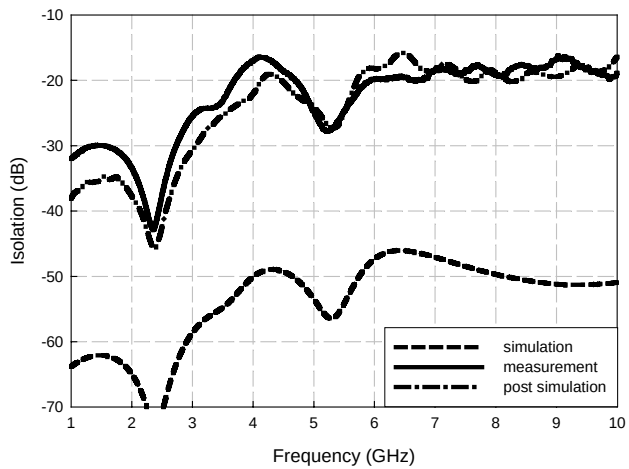


(4) Dual-Band Switch





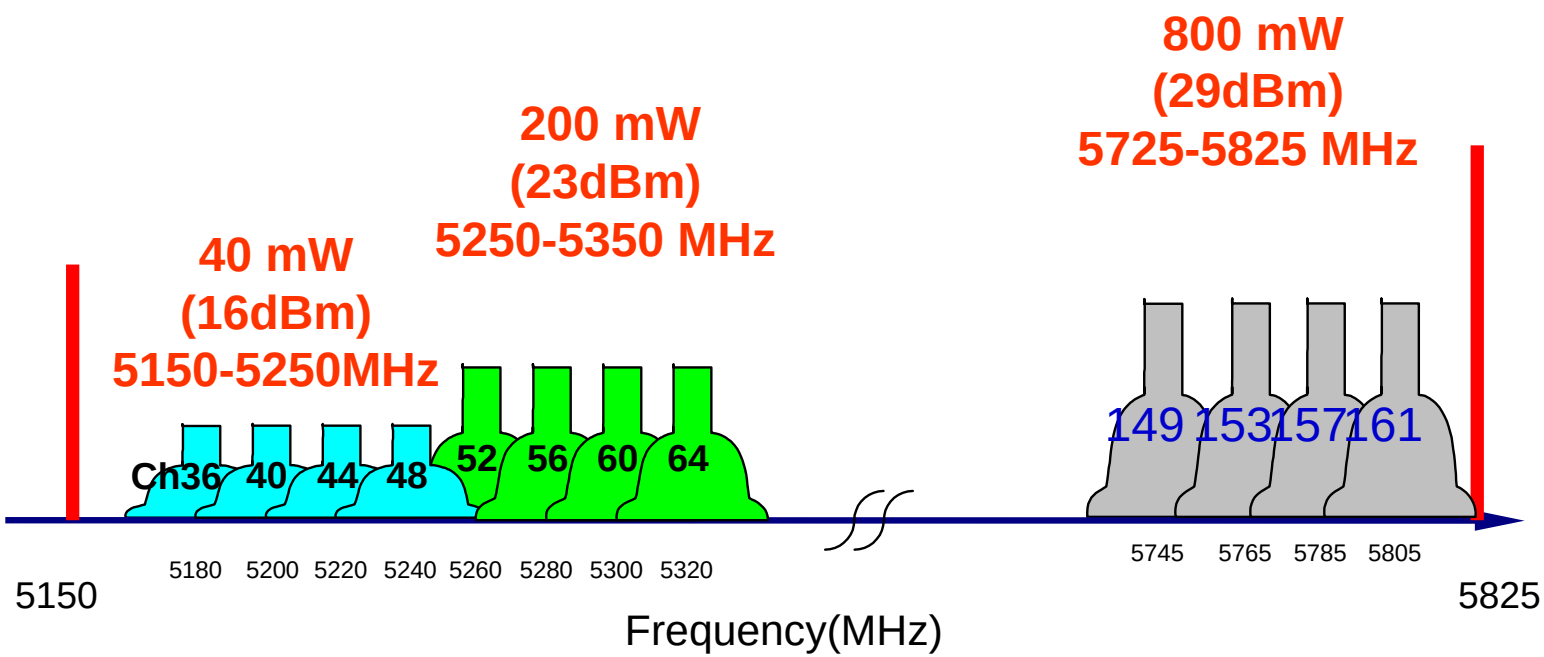




(II) Transmit power levels and spectrum mask

A. Transmit power levels

IEEE802.11a - 17.3.9.1：

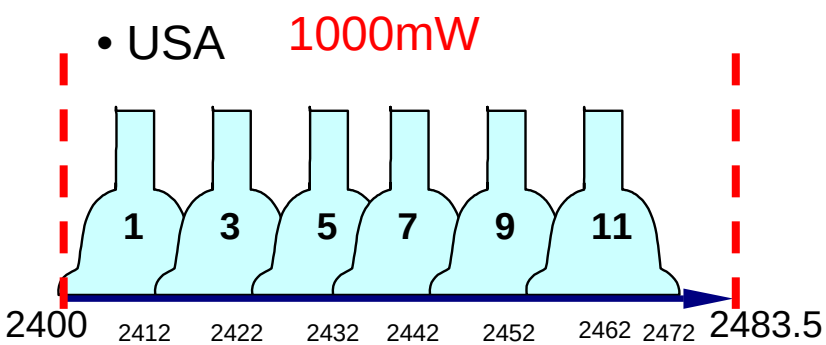


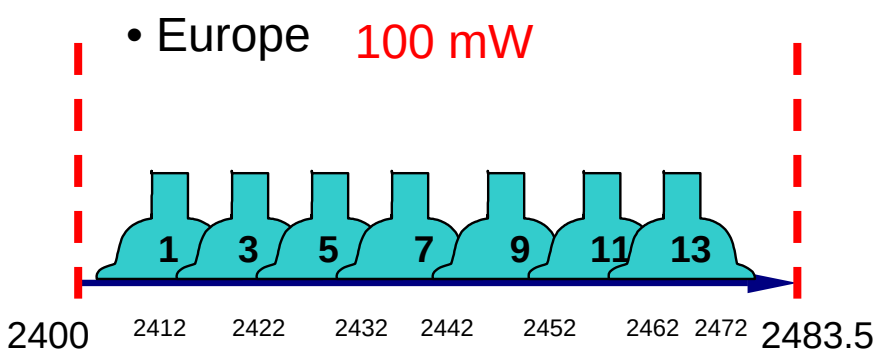
IEEE802.11b - 18.4.7.1：1000mW(USA)

100mW(Europe)

10mW/MHz(Japan)

IEEE802.11g - 19.4.7.1：same as 18.4.7.1





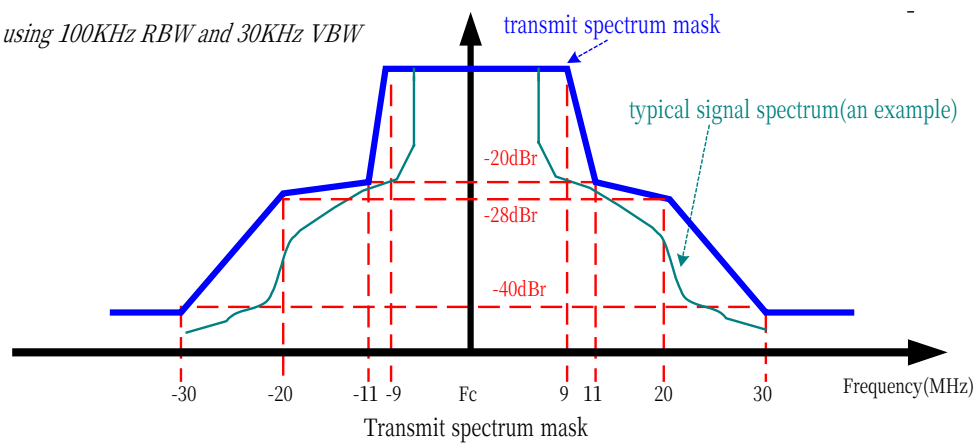
B. Transmit Spectrum Mask

IEEE802.11a：17.3.9.2

IEEE802.11b：18.4.7.3

** The transmitted bandwidth shall have not exceeding 18 MHz*

** using 100KHz RBW and 30KHz VBW*



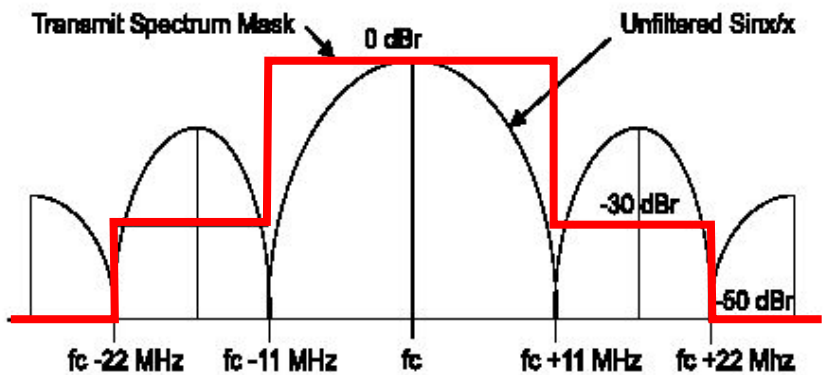
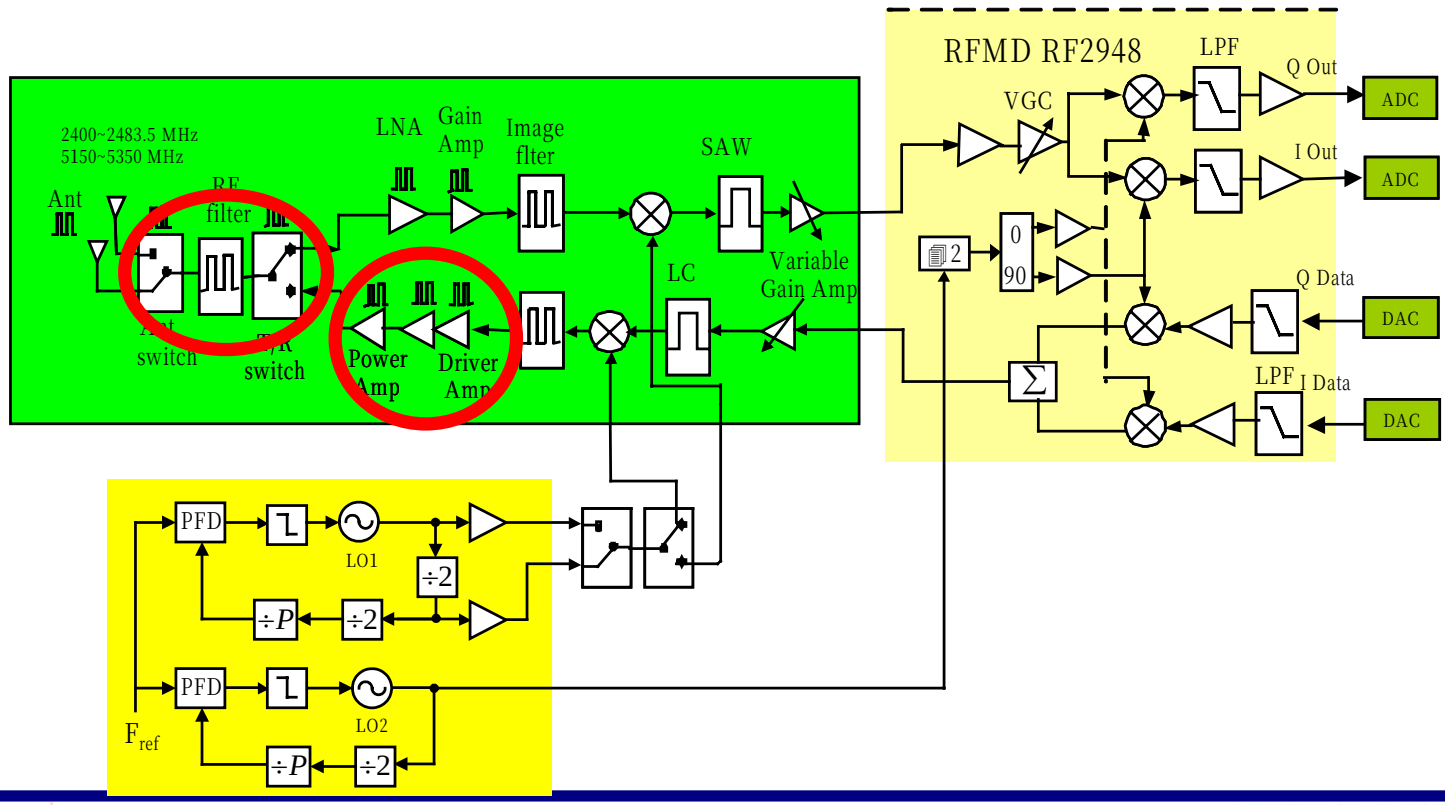
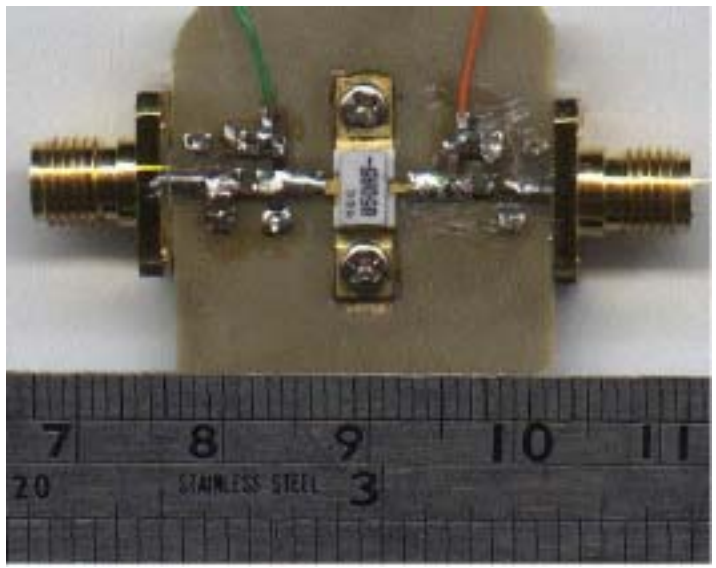


Figure 145—Transmit spectrum mask

Related to Power Amplifier, RF Filter, RF Switch



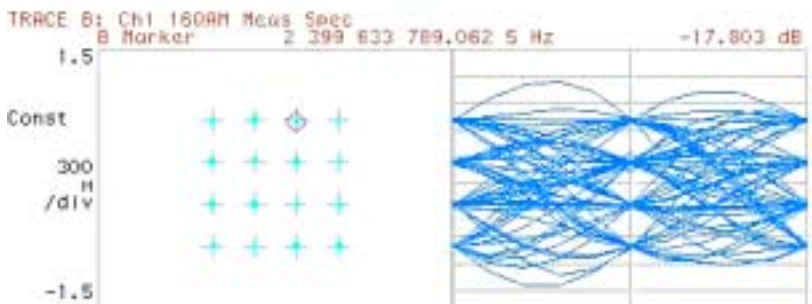
Example: 2.4 GHz Class-AB PA



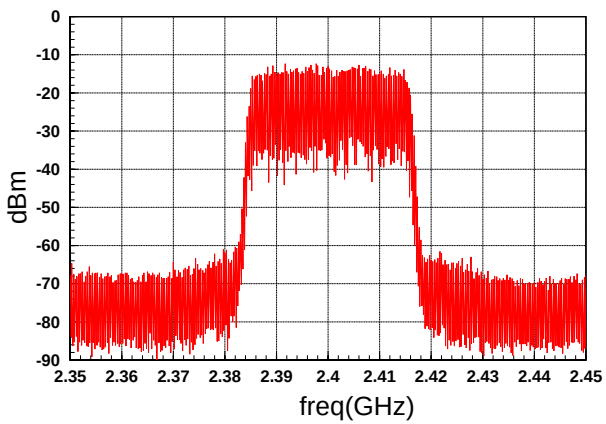
Frequency	2400-2500 MHz
Output P_{1dB}	24.5 dBm
Output IP3	39.5 dBm
Power gain	14dB
Input return loss	>8dB
Output return loss	>10dB
$PAE @ P_{out} = 24dBm$	38%
DC bias	5V;150mA

PA is driven to have **13.5 dBm** output power

EVM=1.3%(-18.8 dB)

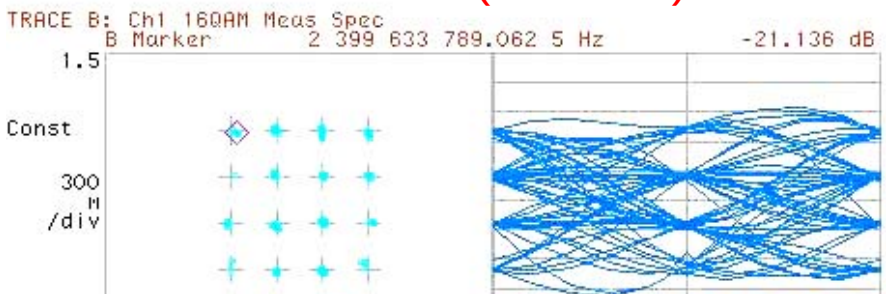


ACPR < -55dBc

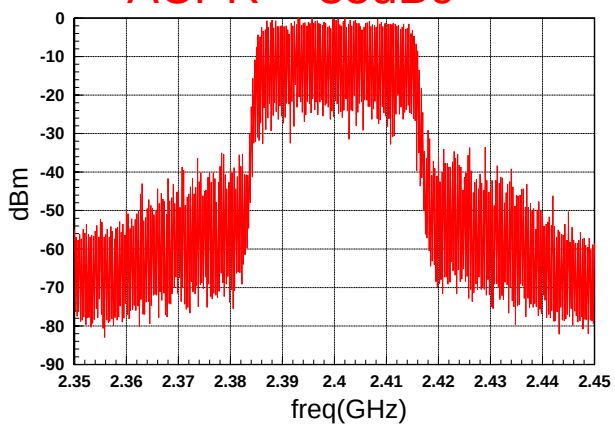


PA is driven to have **22.5 dBm** output power

EVM=4.1%(-13.8 dB)



ACPR< -35dBc



(III) Allowed constellation error and modulation accuracy

A. Allowed relative constellation error

IEEE802.11a：17.3.9.6.3

IEEE802.11b：18.4.7.8

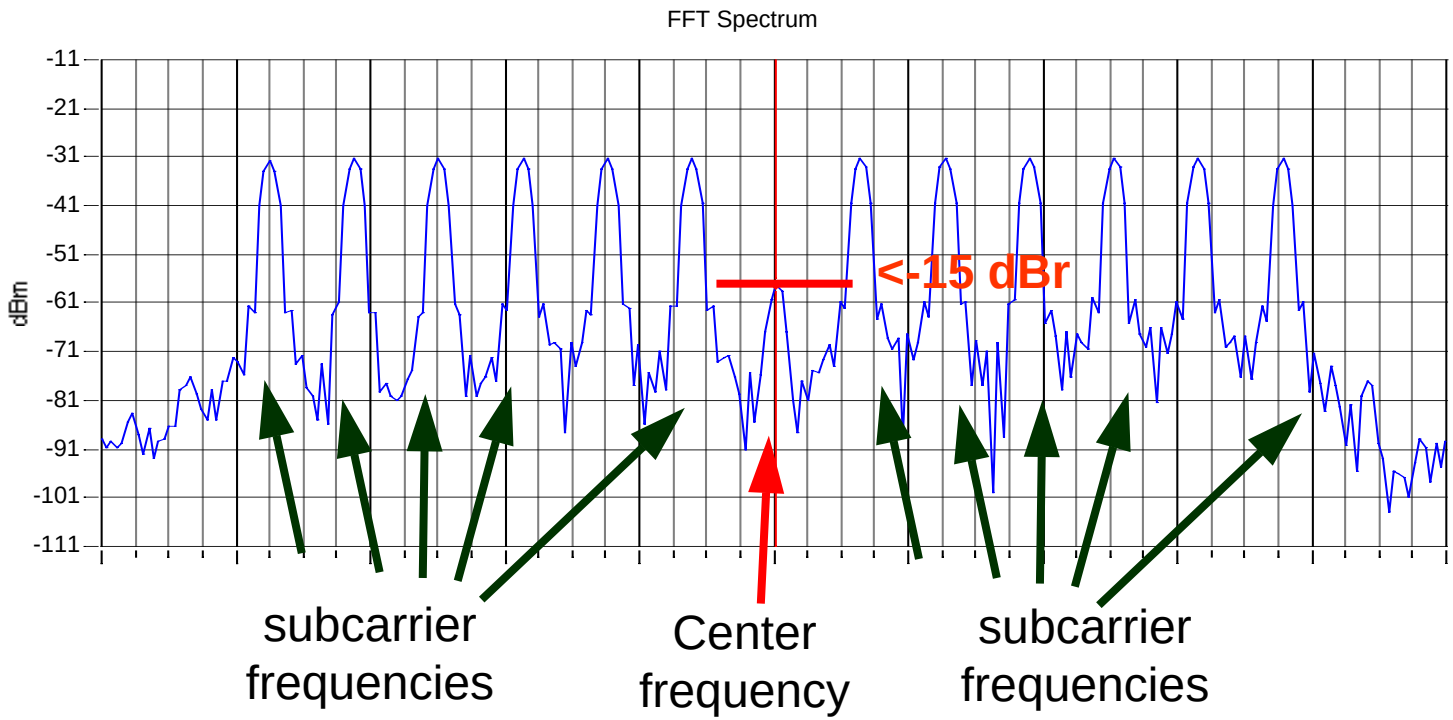
Table 90—Allowed relative constellation error versus data rate

Data rate (Mbits/s)	Relative constellation error (dB)
6	–5
9	–8
12	–10
18	–13
24	–16
36	–19
48	–22
54	–25

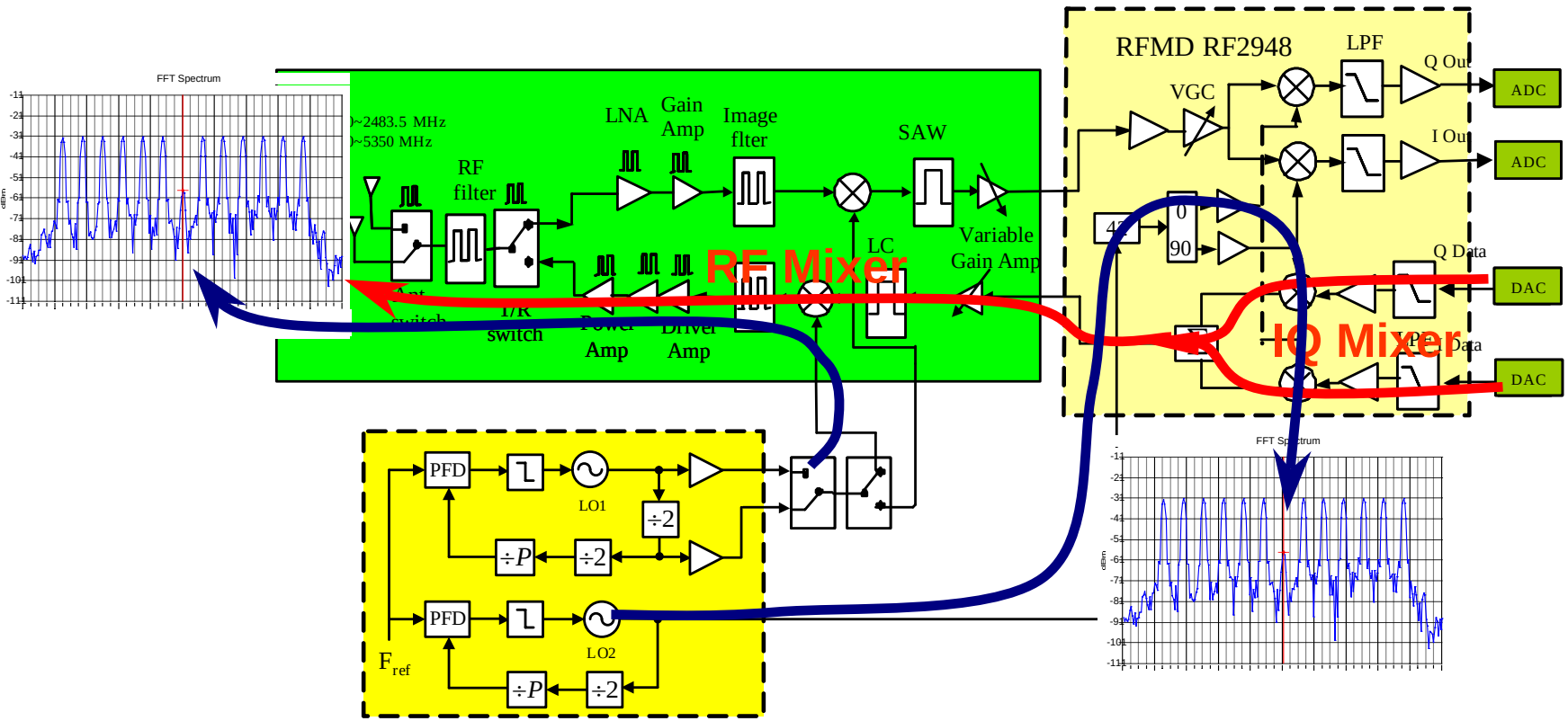
Worst-case vector error magnitude shall not exceeded 0.35 (-4.55dB) for the normalized sampled chip data.

B. Modulation Accuracy

17.3.9.6.1 Transmit Center Frequency Leakage
<-15 dB relative to overall transmitted power
e.g. 23 dBm transmitted power, 8 dBm center leakage power



Related to baseband IQ Mixer, RF mixer



(IV) Receiver Dynamic Range

A. Receiver minimum input level sensitivity

IEEE802.11a：17.3.10.1

Minimum Input Power at the Antenna Connector for Packet Error Rate < 10% at a PSDU length of 1000 bytes

Data Rate (bits/s)	Minimum power at antenna port (dBm)
6	**-82**
9	**-81**
12	**-79**
18	**-77**
23	**-74**
36	**-70**
48	**-66**
54	**-65**

IEEE802.11b：18.4.8.1

-76 dBm at antenna port for frame error ratio (FER)<8% at a PSDU length of 1024 octets. This FER shall be specified for 11 Mbit/s CCK modulation

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Center for Telecommunication Research

B. Receiver Maximum Input level

IEEE802.11a：17.3.10.4

- **–30 dBm measured at the antenna connector for a maximum Packet Error Rate < 10% at a PSDU length of 1000 bytes**

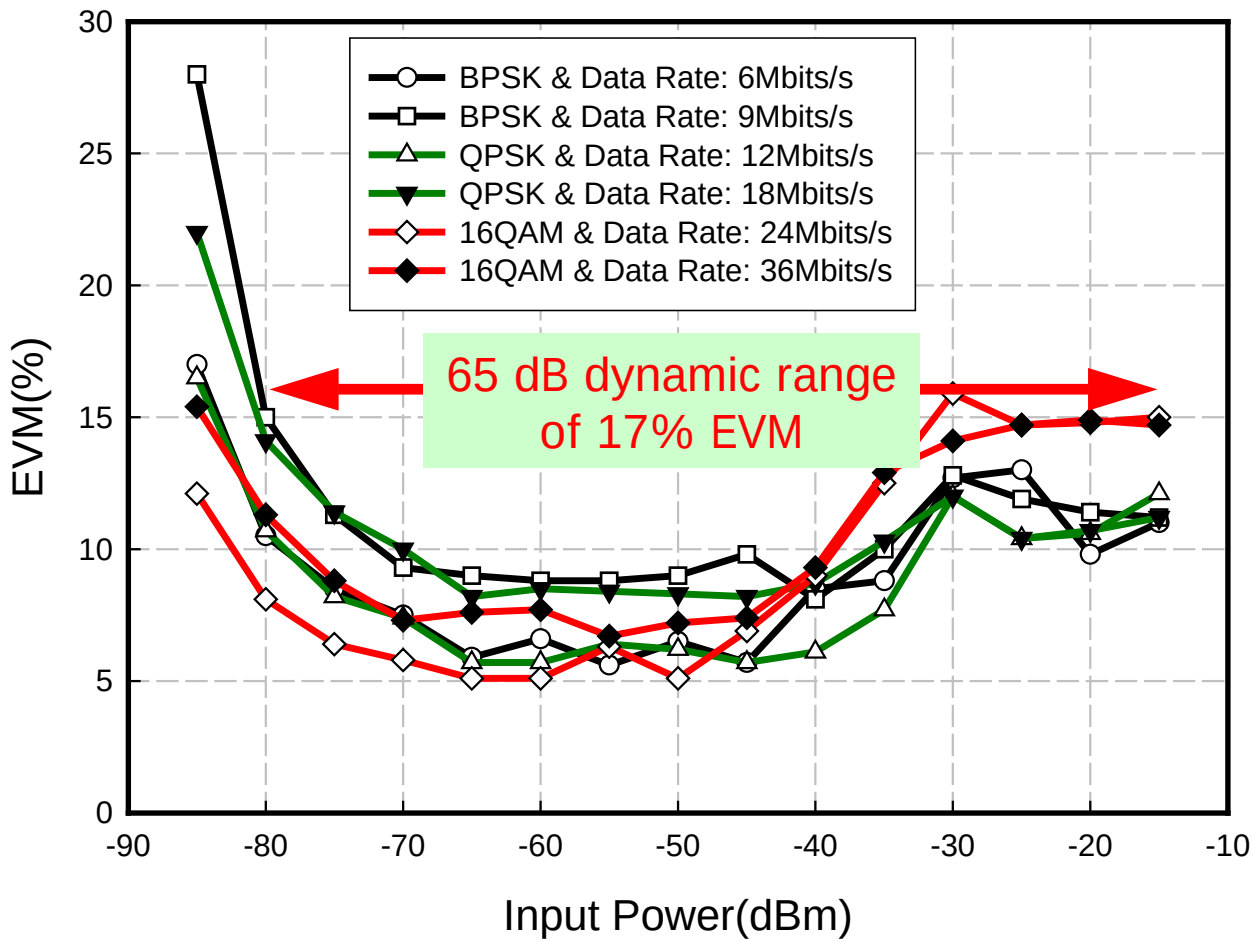
IEEE802.11b：18.4.8.2

- **–10 dBm measured at the antenna for a maximum FER of 8% at a PSDU length of 1024 octets.**
- **This FER shall be specified for 11 Mbit/s CCK modulation.**

IEEE802.11g：19.5.3

–20 dBm measured at the antenna connector for the PER less than 10% at a PSDU length of 1000 bytes for any supported modulation signal or data rate (i.e., 1, 2, 5.5, 6, 9, 11, 12, 18, 22, 24, 33, 36, 48, 54 Mbit/s).

EVM Measurement by HP89441



(V) Adjacent Channel Rejection

A. Adjacent Channel Rejection

IEEE802.11a：17.3.10.2

Interfering Signal Power at Adjacent Channel, referenced to the Desired Signal Level set at 3 dB above the Sensitivity, for Packet Error Rate < 10% at a PSDU length of 1000 bytes

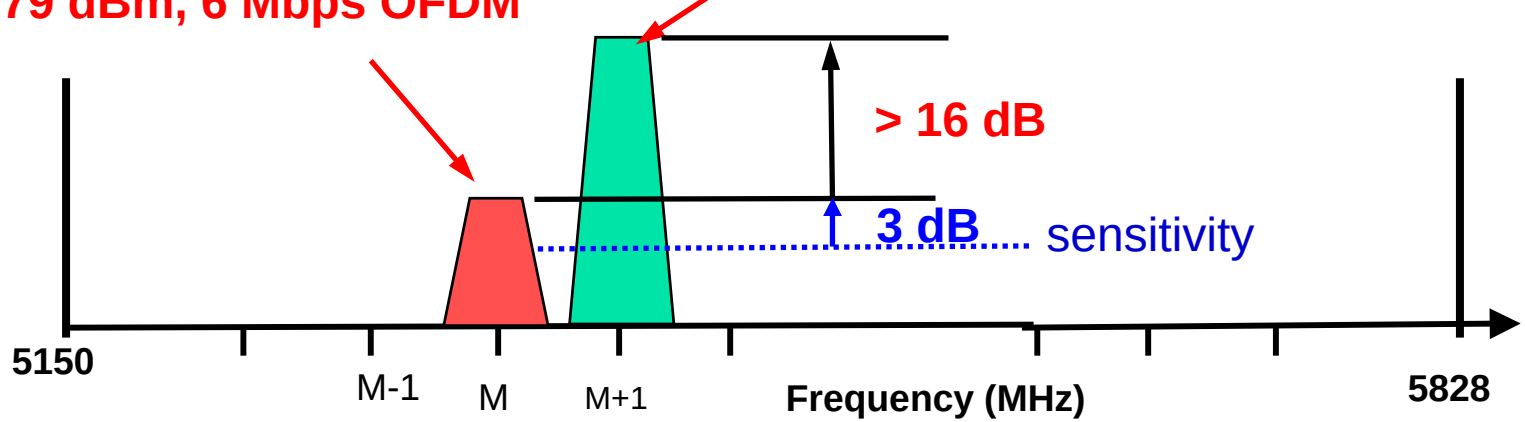
For example:

Desired Signal :

-79 dBm, 6 Mbps OFDM

Adjacent Signal :

6 Mbps OFDM



IEEE802.11b：18.4.8.3

The adjacent channel rejection shall be equal to or better than 35 dB, with an FER of 8×10–2 using 11 Mbit/s CCK modulation and a PSDU length of 1024 octets.

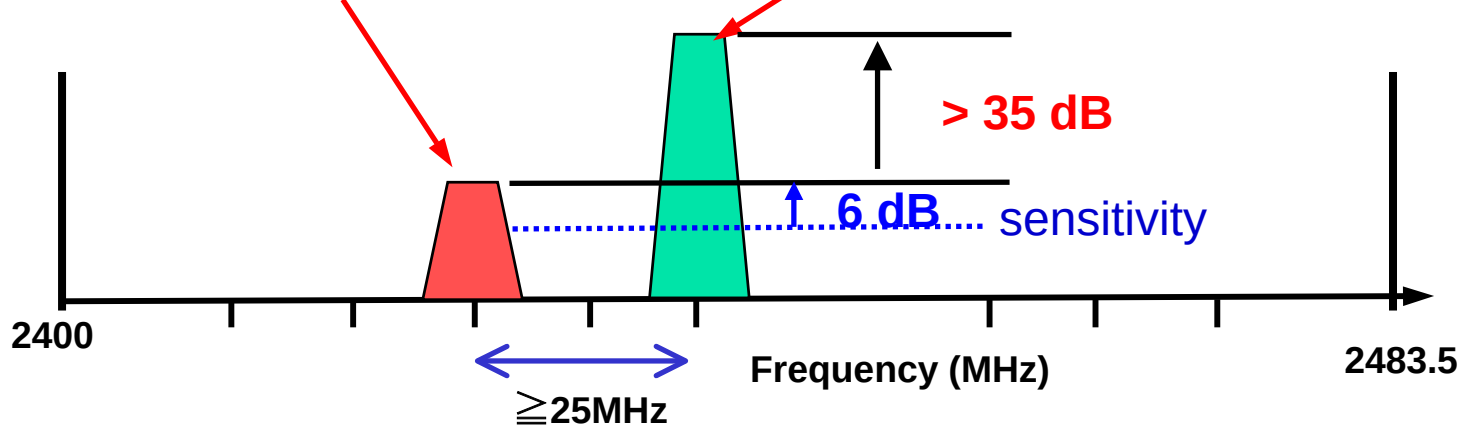
For example:

Desired Signal :

-70 dBm, 11 Mbps CCK

adjacent Signal :

11 Mbps CCK



IEEE802.11g: 19.5 ERP operation specifications

19.5.2 Adjacent channel rejection

For an OFDM PHY the corresponding rejection shall be no less than specified in Table 91 of 17.3.10.(IEEE802.11a)

The adjacent channel rejection of the ERP-DSSS modes shall follow 18.4.8.3 (IEEE802.11b)

19.6 ER-PBCC operation specifications

19.6.2 Receiver adjacent channel rejection

The adjacent channel rejection shall be equal to or better than 35 dB, with an FER of 8×10^{-2} using ER-PBCC modulation and a PSDU length of 1024 octets

B. Non-adjacent Channel Rejection

Interfering Signal Power at Non-adjacent Channel, referenced to the Desired Signal Level set at 3 dB above the Sensitivity, for Packet Error Rate < 10% at a PSDU length of 1000 bytes

Table 91—Receiver performance requirements

Data rate (Mbits/s)	Minimum sensitivity (dBm)	Adjacent channel rejection (dB)	Alternate adjacent channel rejection (dB)
6	–82	16	32
9	–81	15	31
12	–79	13	29
18	–77	11	27
24	–74	8	24
36	–70	4	20
48	–66	0	16
54	–65	–1	15

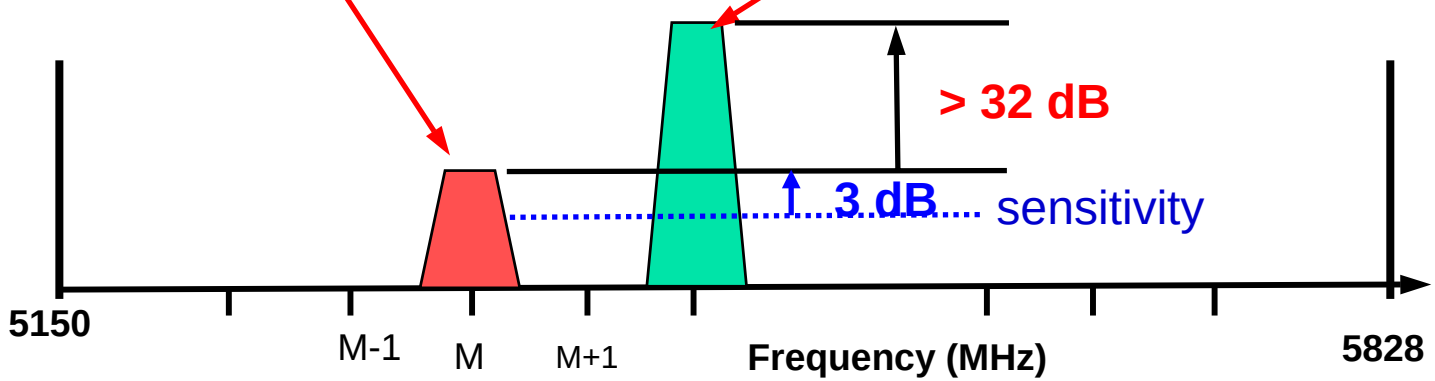
For example:

Desired Signal :

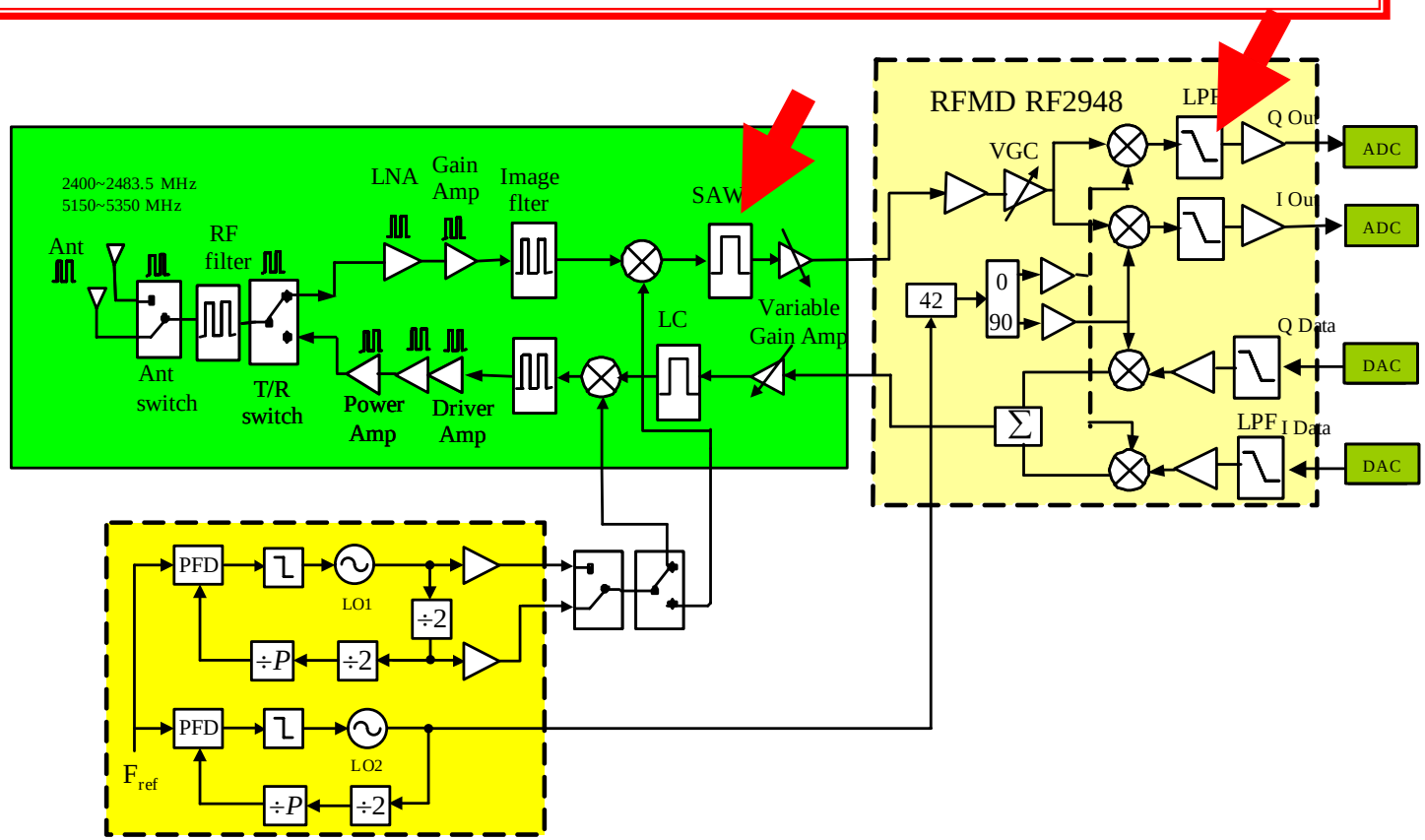
-79 dBm, 6 Mbps OFDM

Non-adjacent Signal :

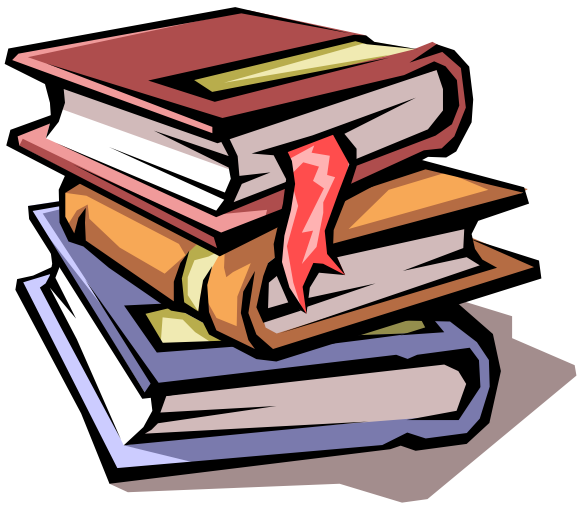
6 Mbps OFDM

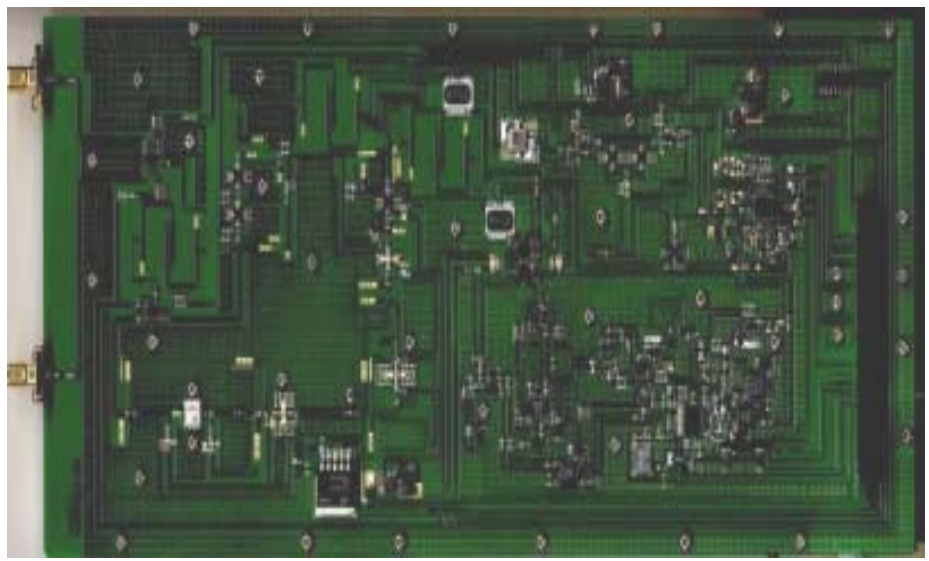


Related to Channel Selection Filter(IF SAW, Baseband Digital Filter)



How do we achieve?





III. Design Example: Dual-Band WLAN RF Module

(A) RF Transceiver Architecture and Frequency Plan

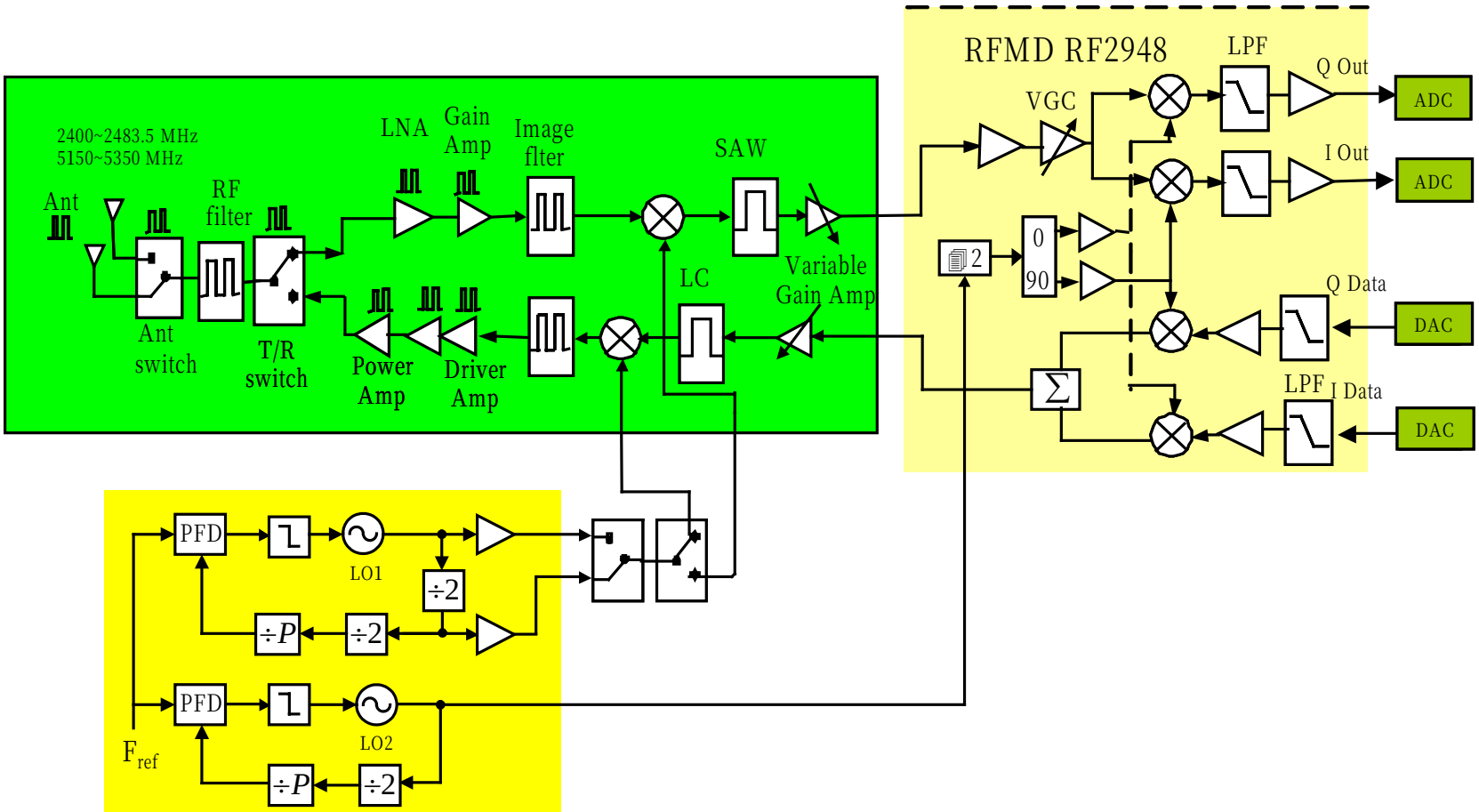
(B) Transmitter Power Budget

(C) Receiver Gain Budget

(D) Key Components Design

(E) Module Integration

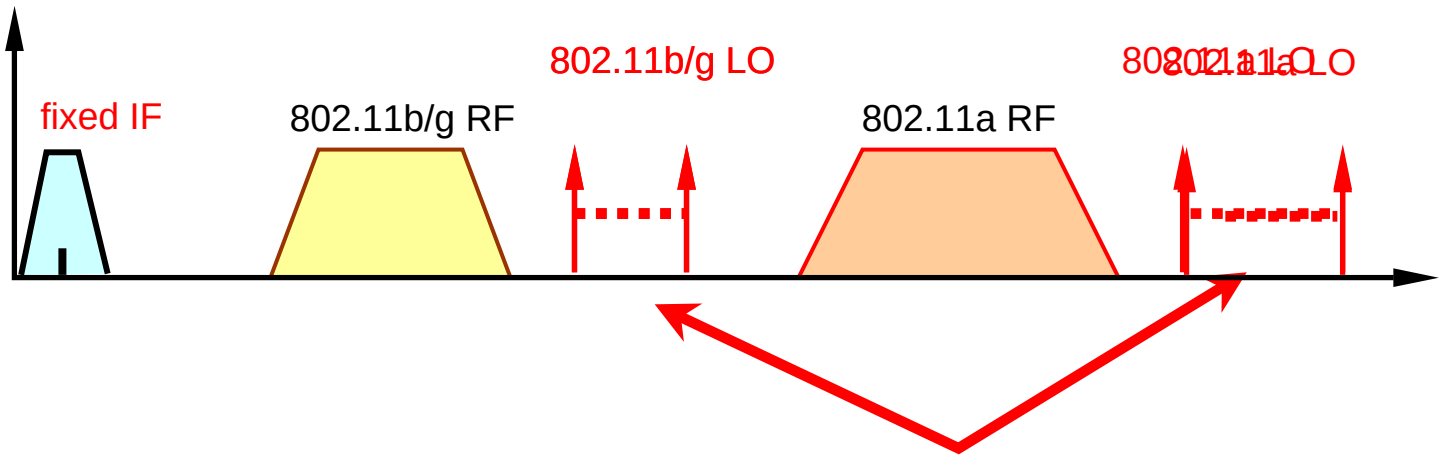
(A) RF Transceiver Architecture and Frequency Plan



Frequency Planning for 802.11a/b/g RF Transceiver

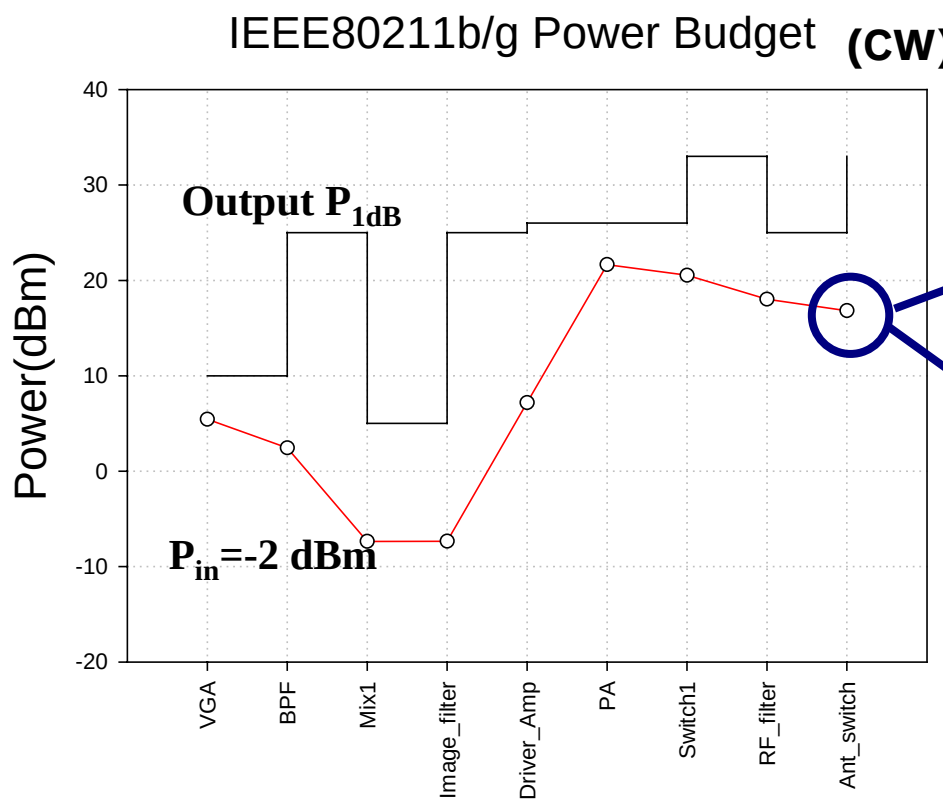
(a) fixed IF or floating IF

(b) LO frequency range

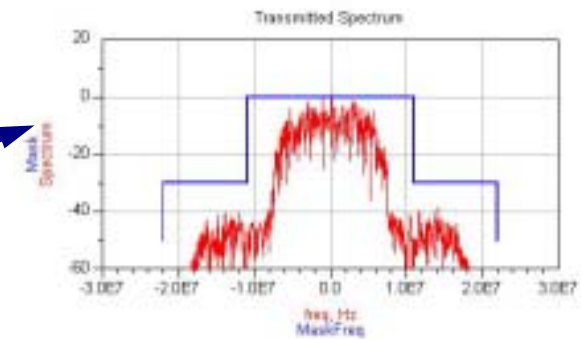


Share same frequency synthesizer to save component count and DC power consumption

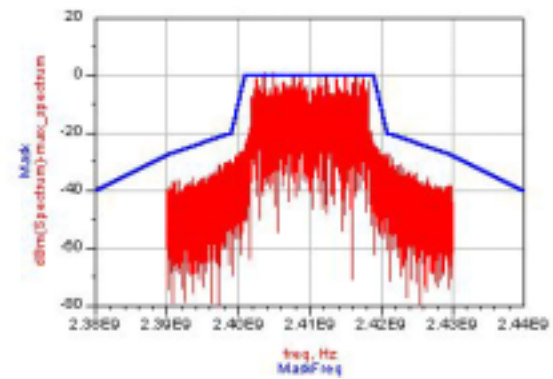
(B) Transmitter Power Budget

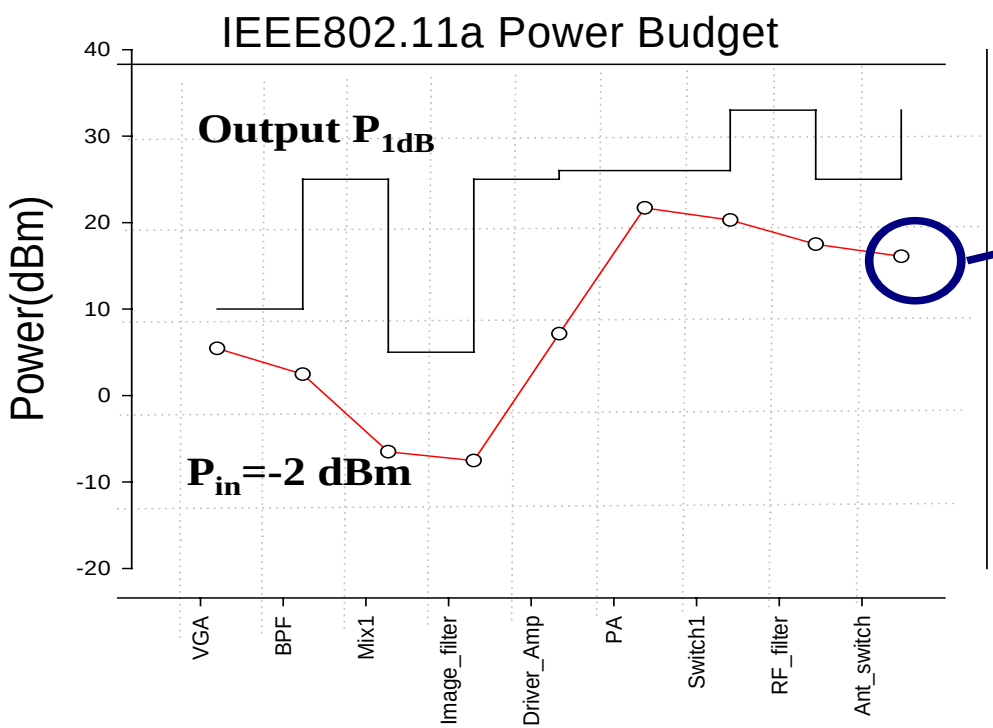


11 Mbps DQPSK

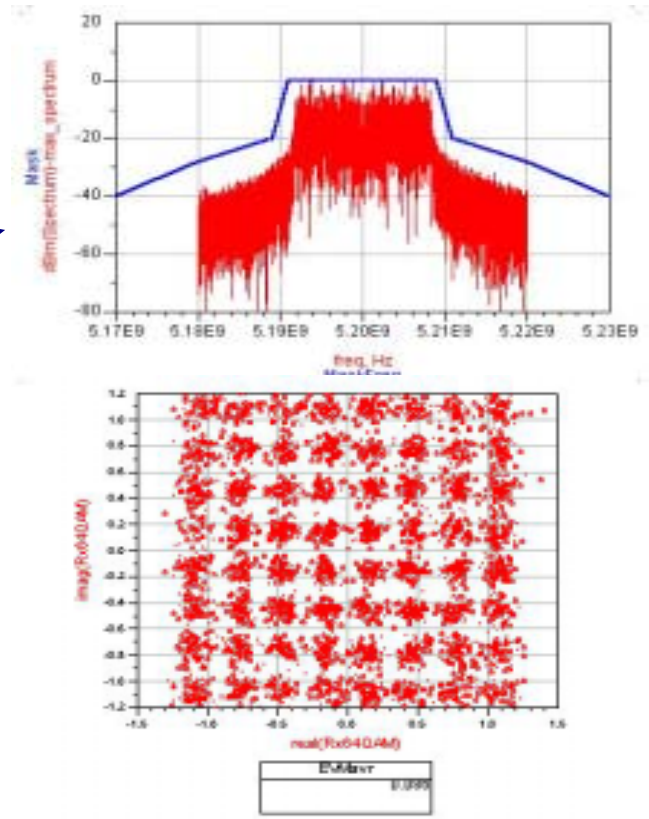


OFDM 54 Mbps 64QAM

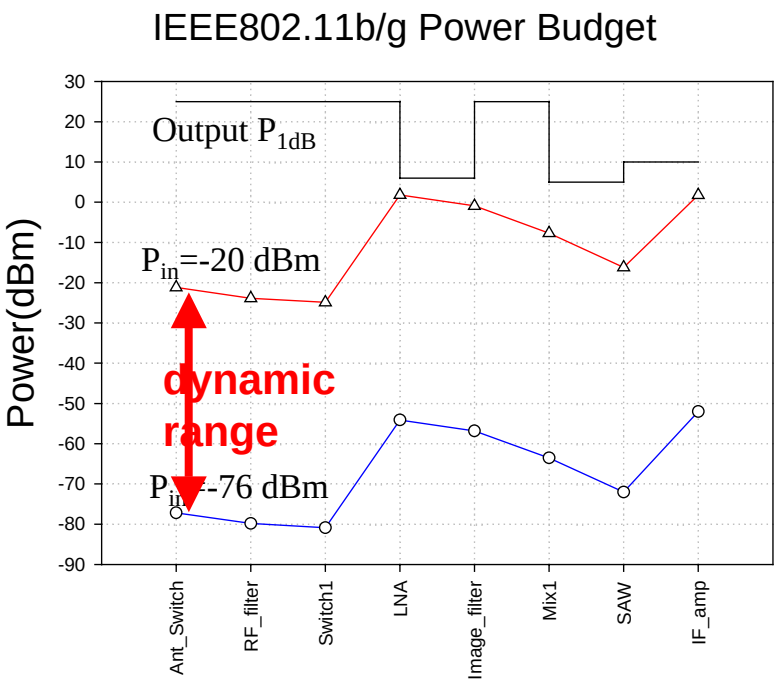


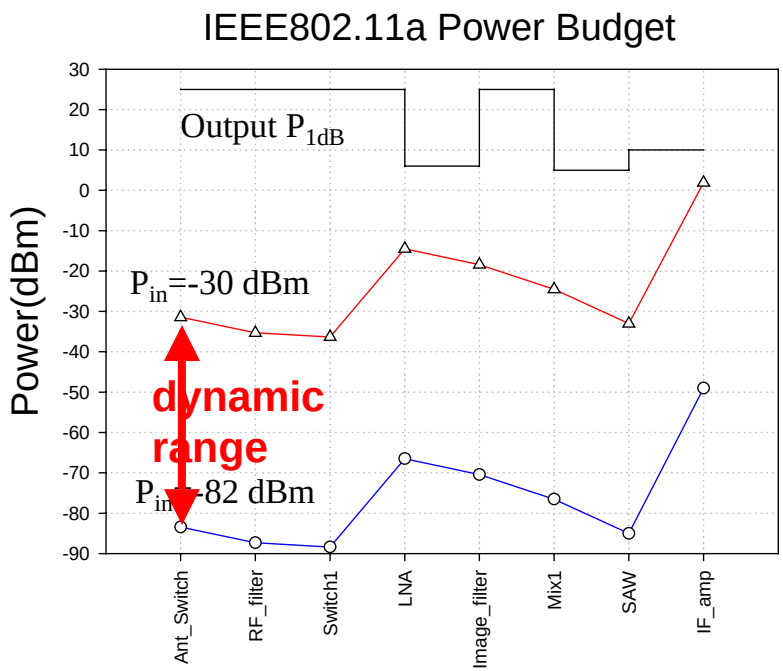


OFDM 54 Mbps 64QAM



(C) Receiver Gain Budget

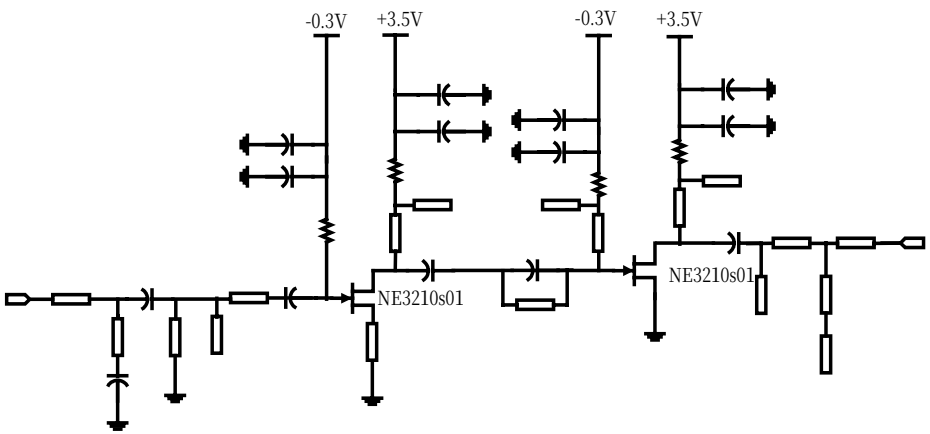


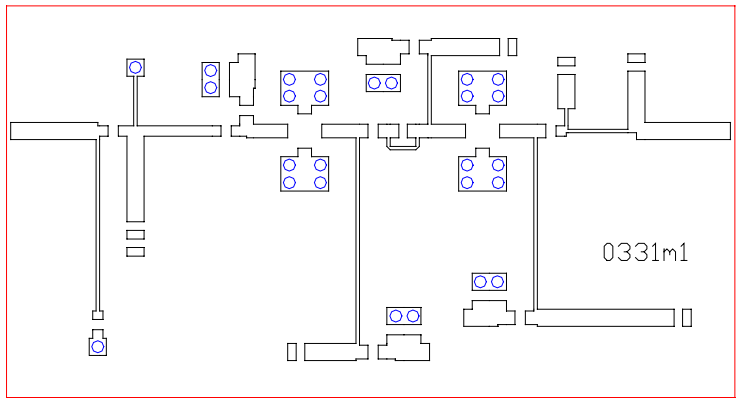


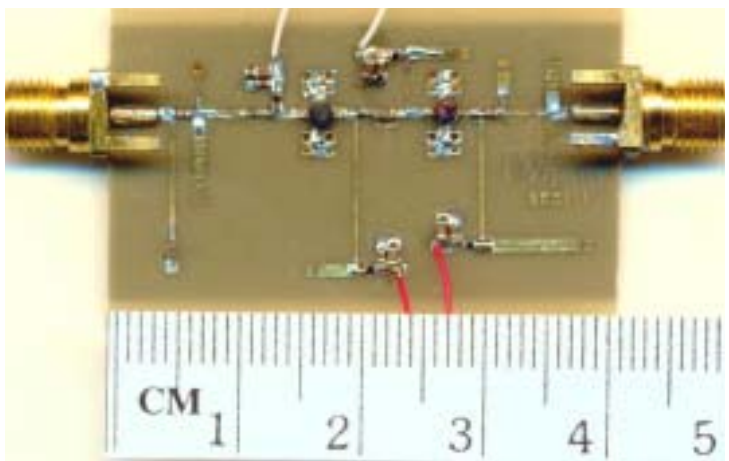
(D) Dual-Band RF Key Component Design

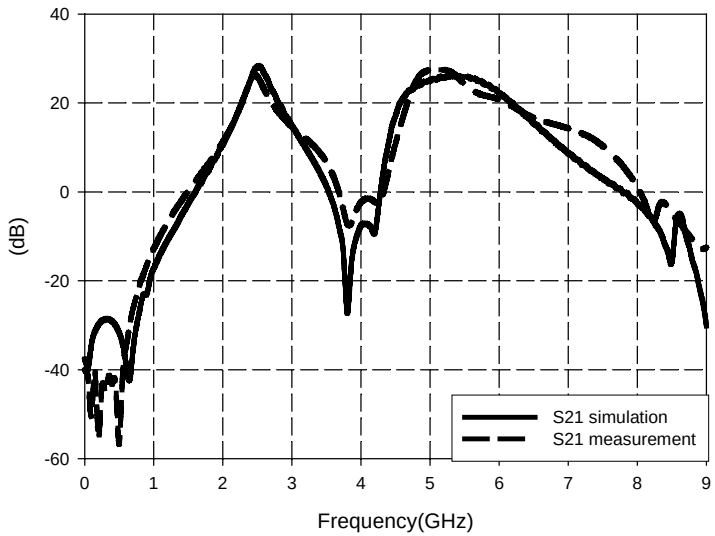
- Concurrent Dual-band LNA
- Concurrent Dual-band PA
- Concurrent Dual-Band Filter
- Concurrent Dual-Band Switch
- VCO and Frequency Synthesizer

(1) Concurrent Dual-Band LNA- Circuit 1

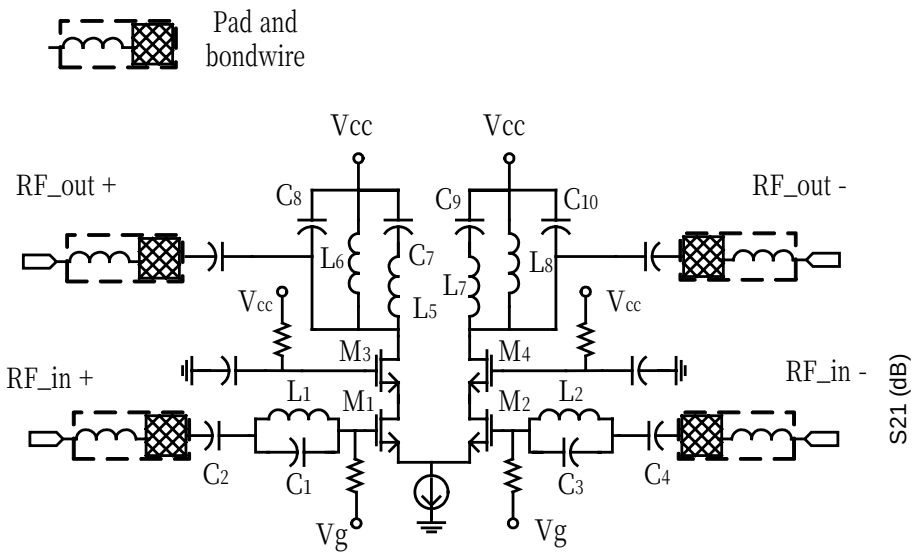


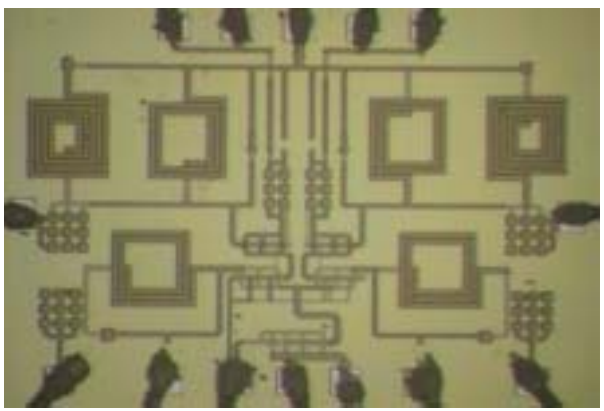


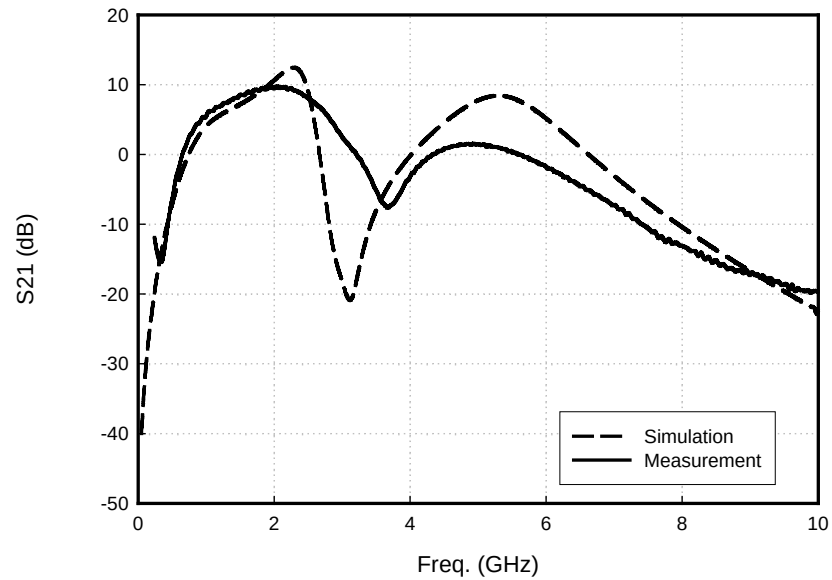




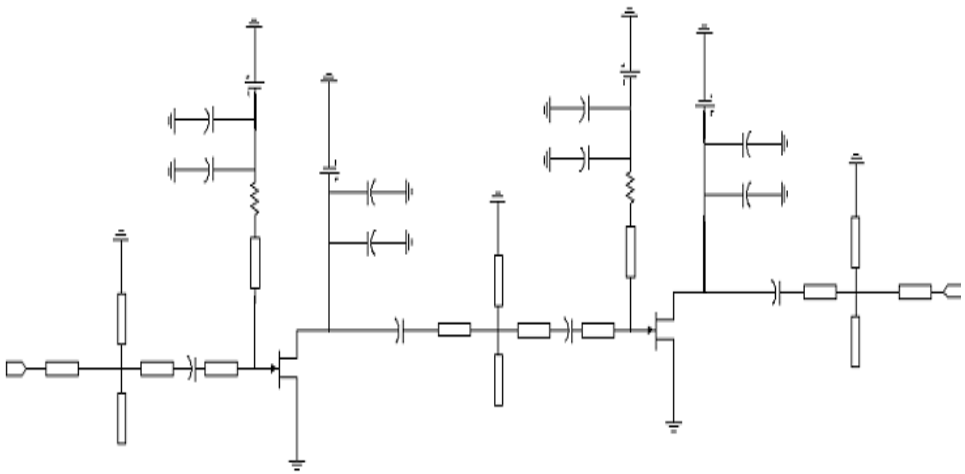
(1) Concurrent Dual-Band LNA- 0.18umCMOS

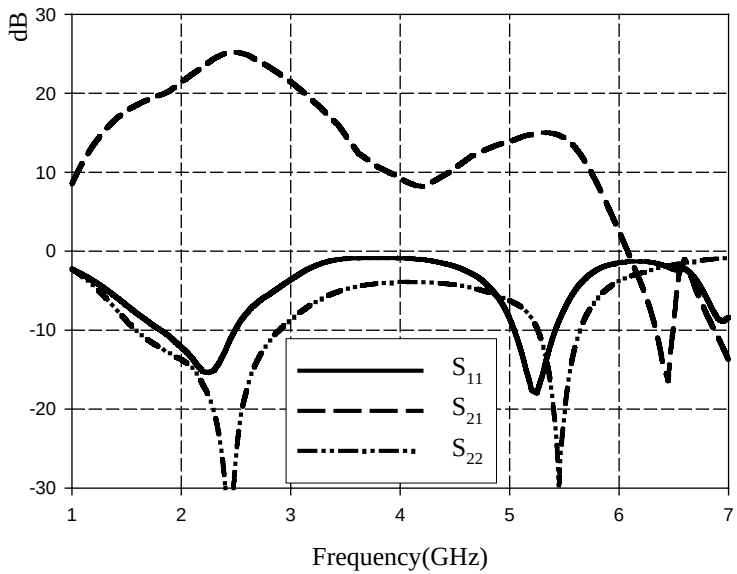


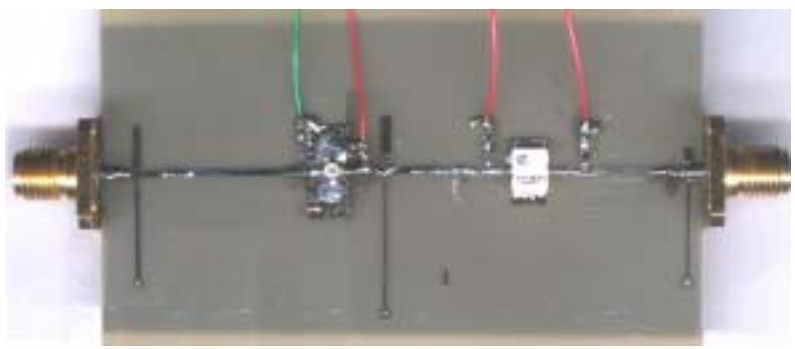




(2) Dual-Band PA

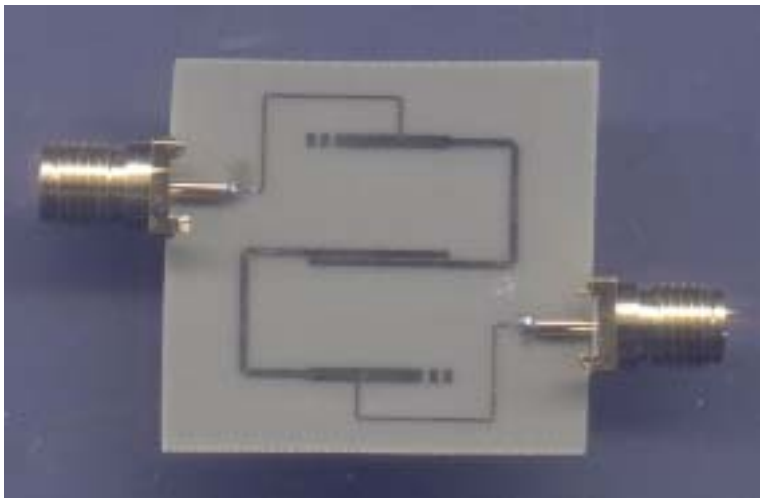


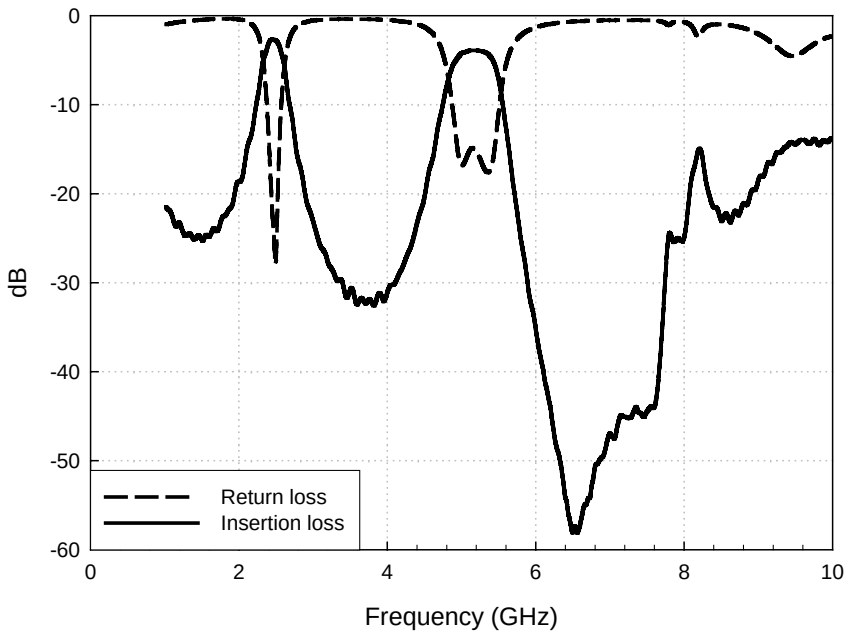




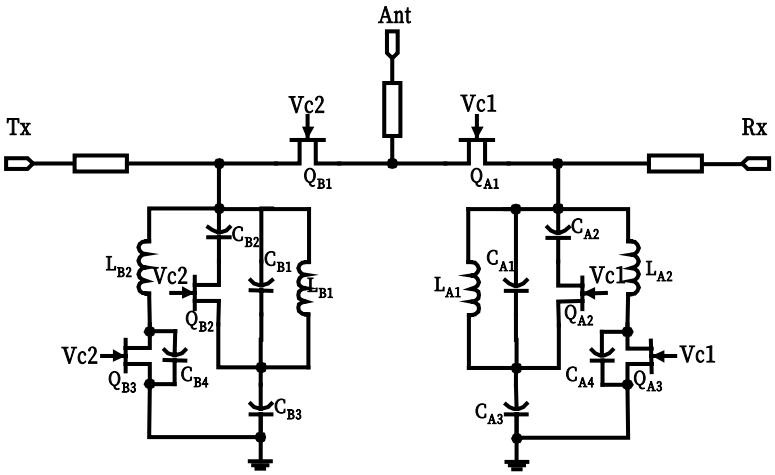
(3) Dual-Band Filter

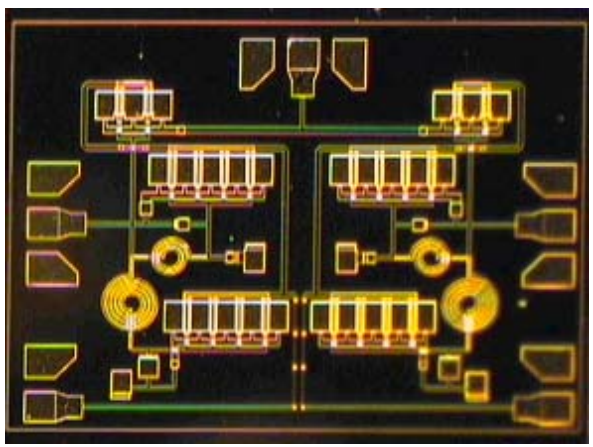
Second-order SIR filter

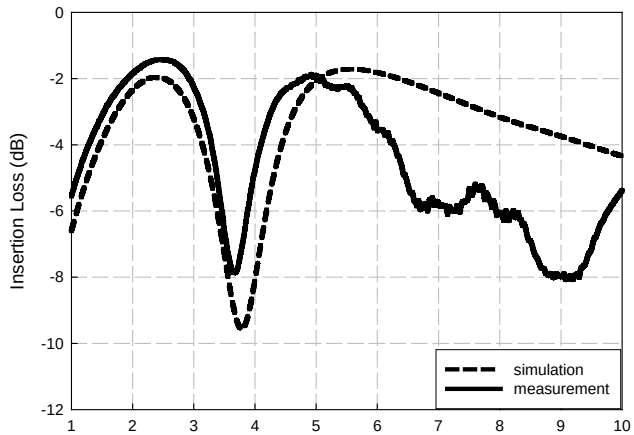


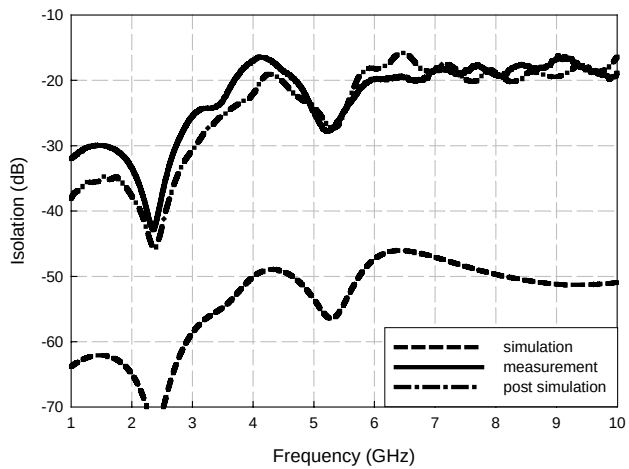


(4) Dual-Band Switch





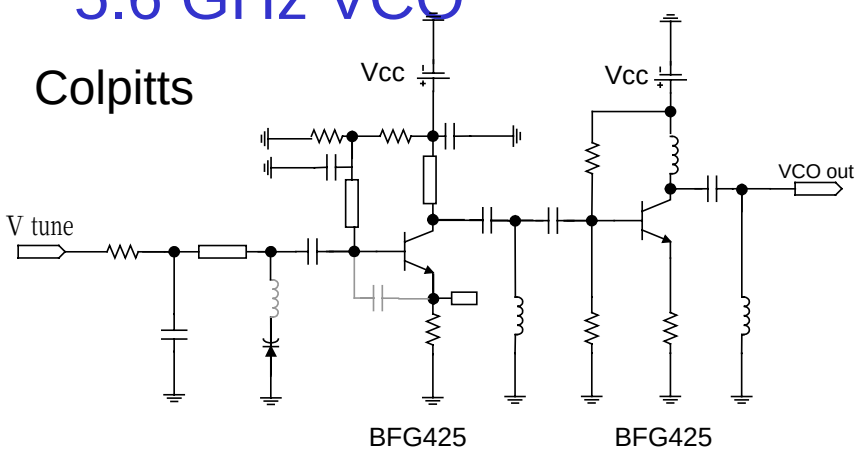


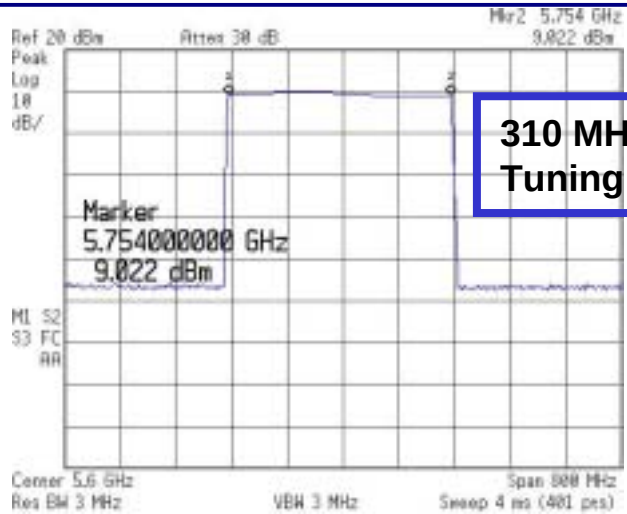


(5) Dual-Band VCO and Frequency Synthesizer

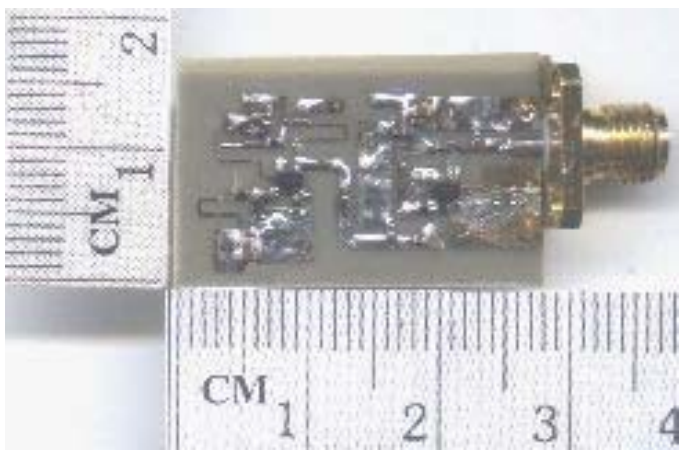
5.6 GHz VCO

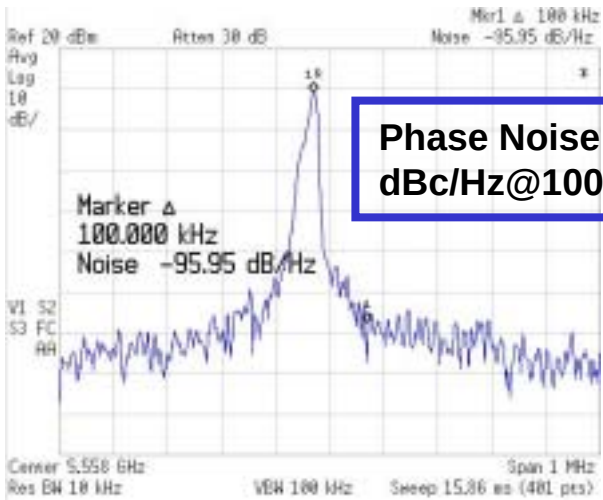
Colpitts





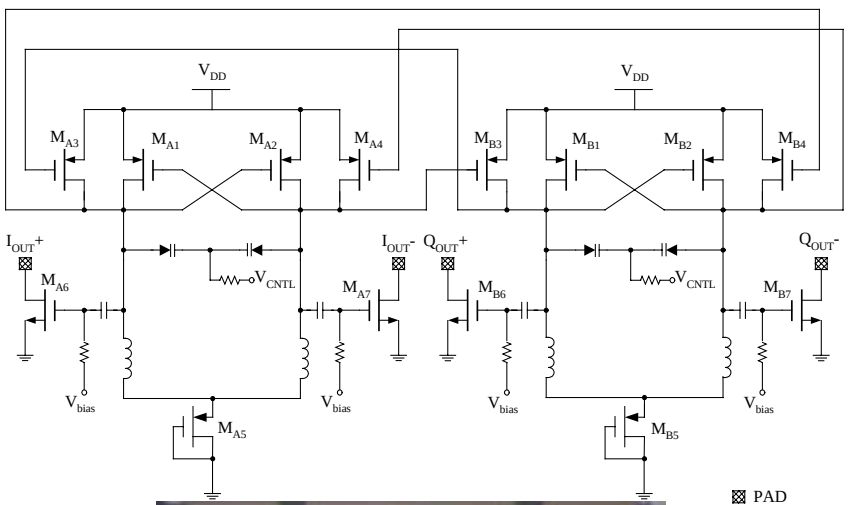
310 MHz Tuning Range

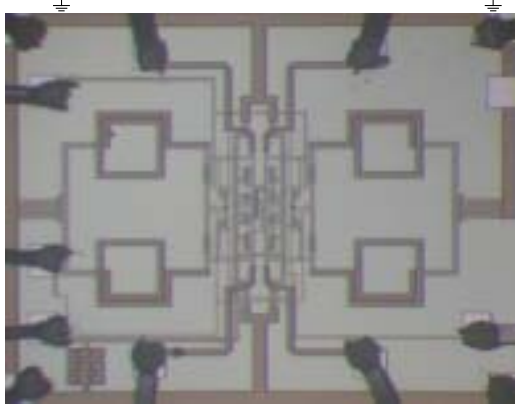




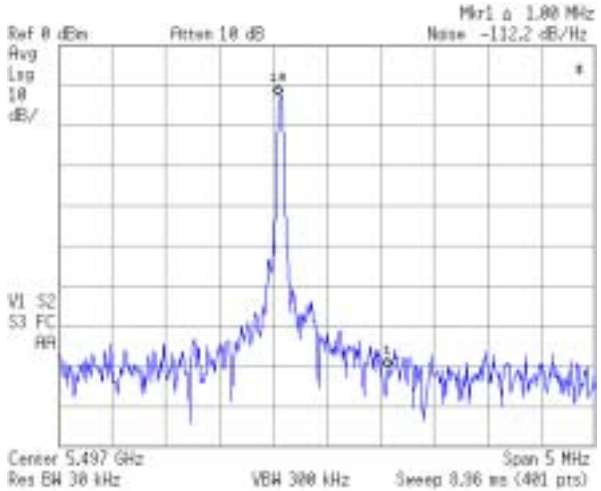
Phase Noise: -95.95 dBc/Hz@100kHz offset

5.6 GHz 0.18um CMOS quadrature VCO

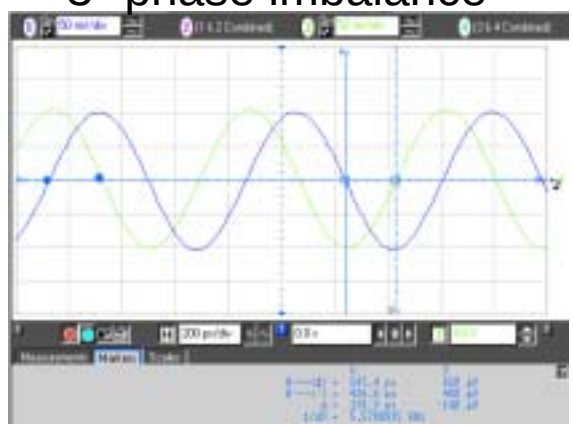


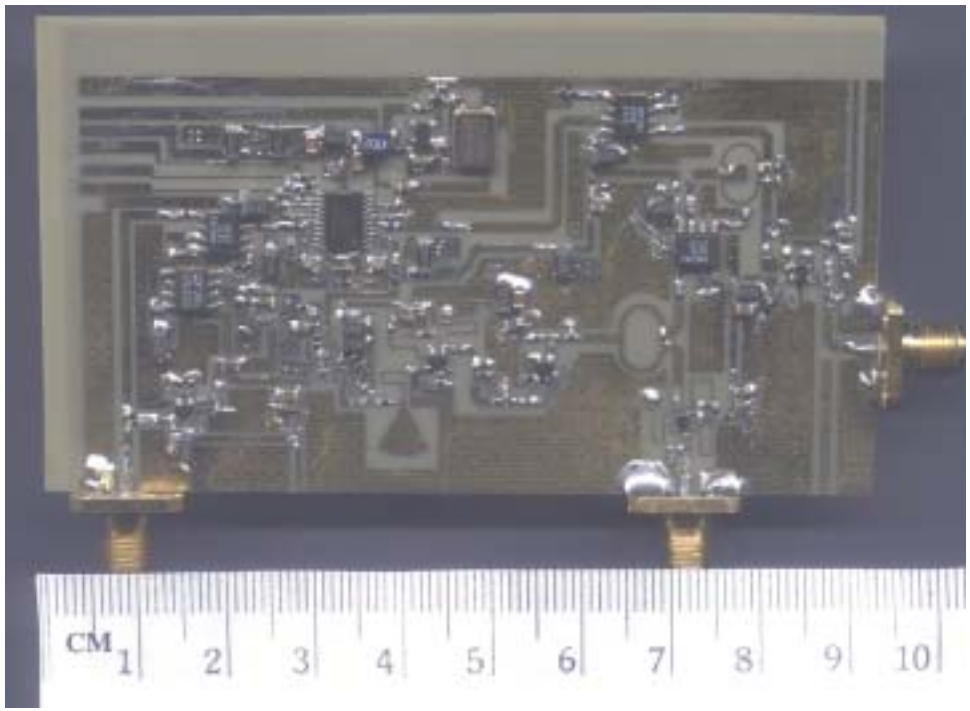


-113 dBc/Hz at 1 MHz off

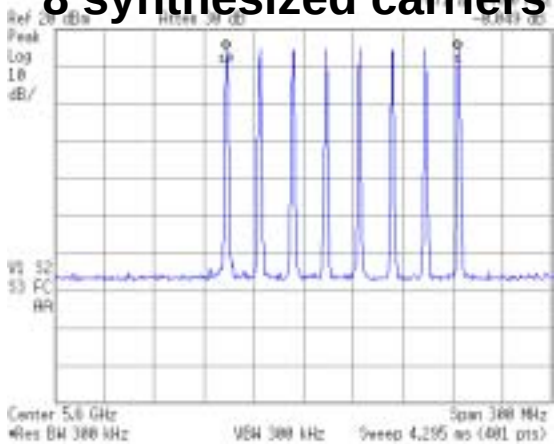


3º phase imbalance

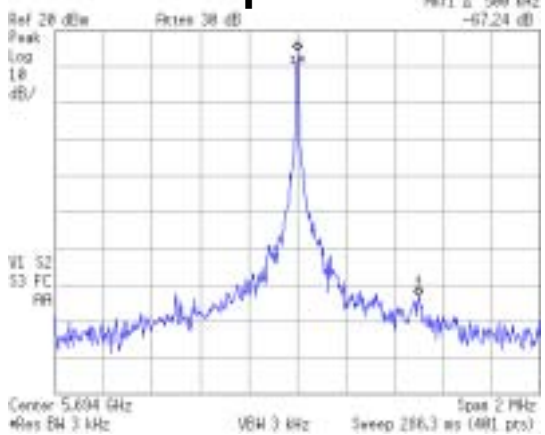




8 synthesized carriers

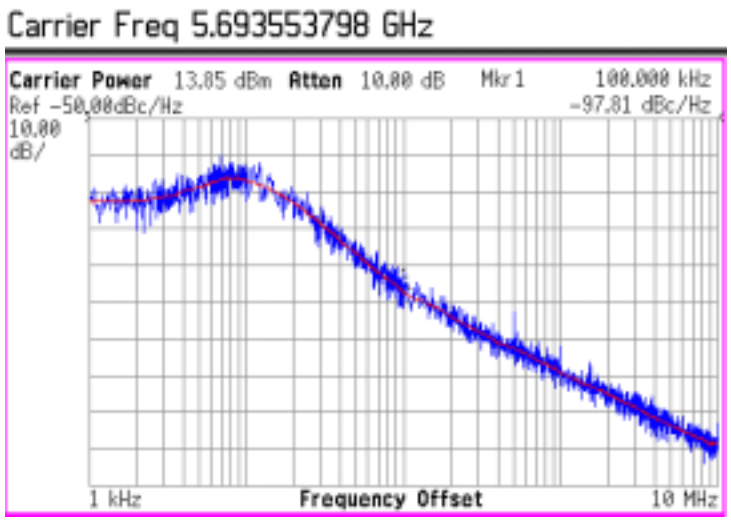


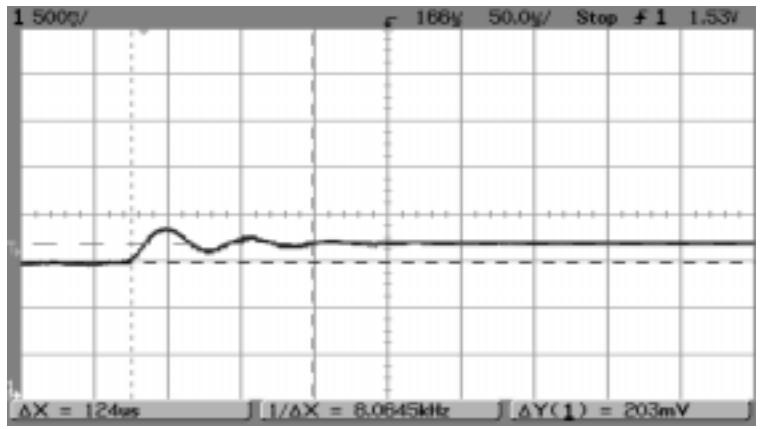
-67 dBC spur level



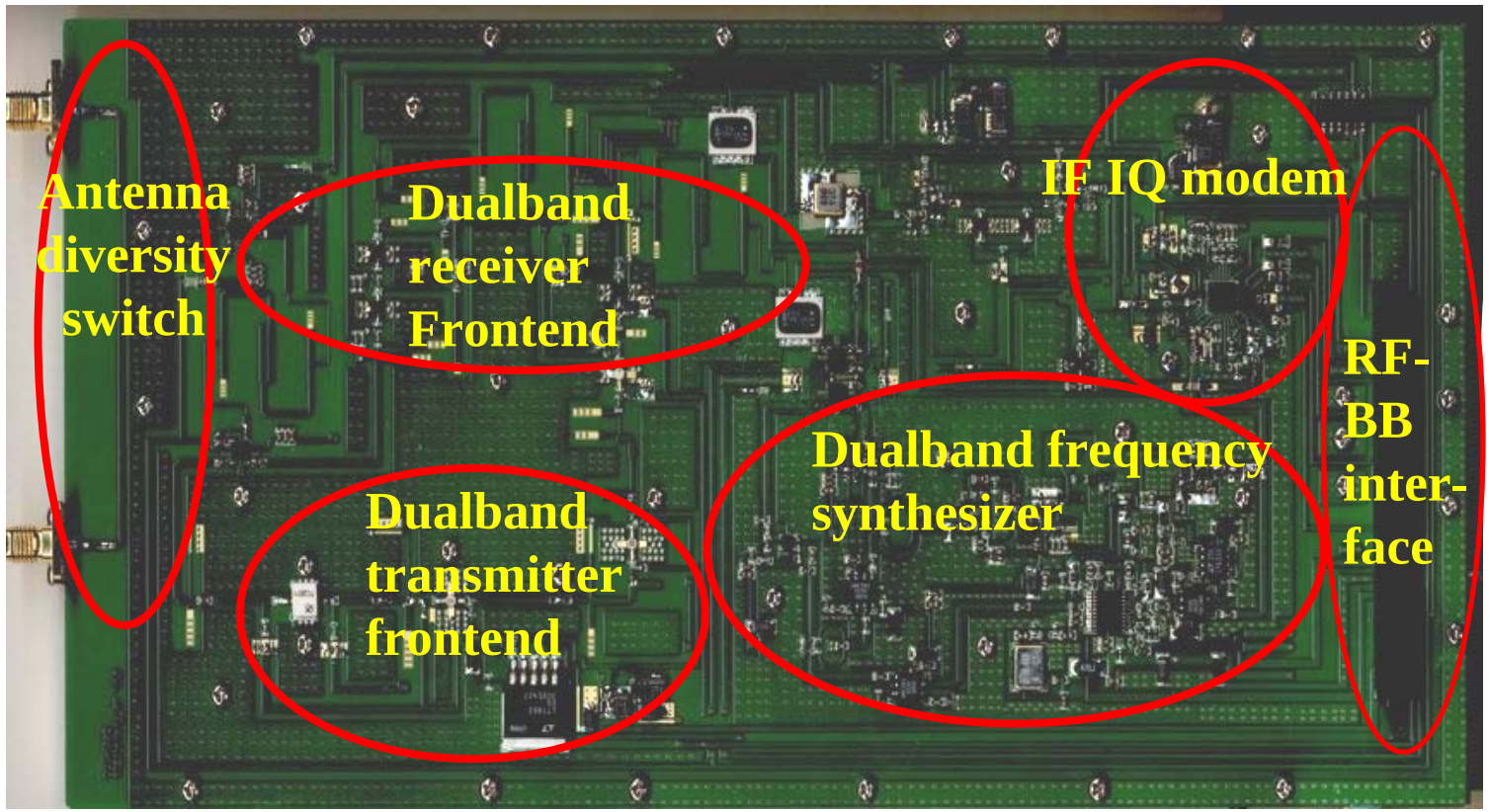
-97.8 dBc/Hz phase noise at 100 kHz off carrier

124 μS settling time





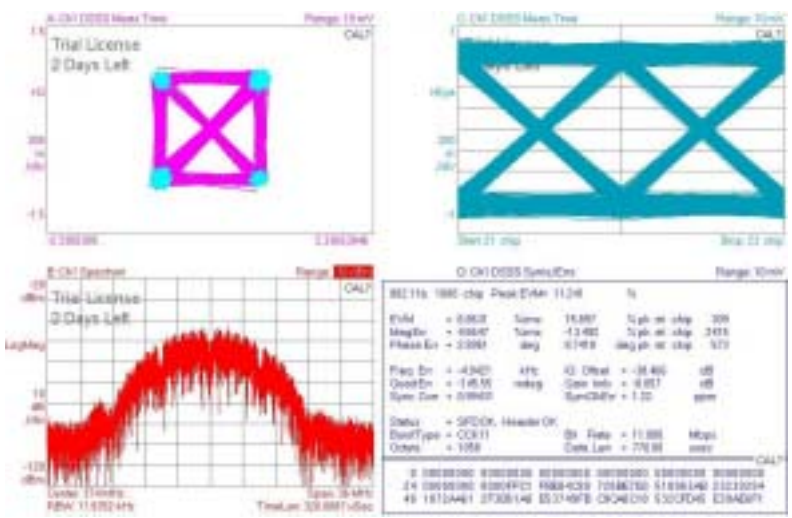
(E) 2.4/5.2-GHz RF Integration



(I) 2.4/5.2-GHz RF receiver test

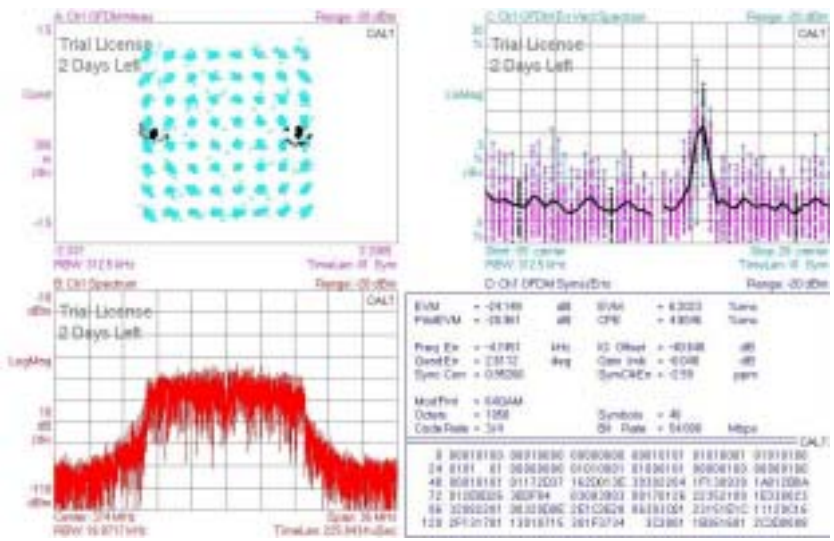
2.4 GHz CCK QPSK 11 Mbps:

EVM=6.86 % (-60dBm received power)



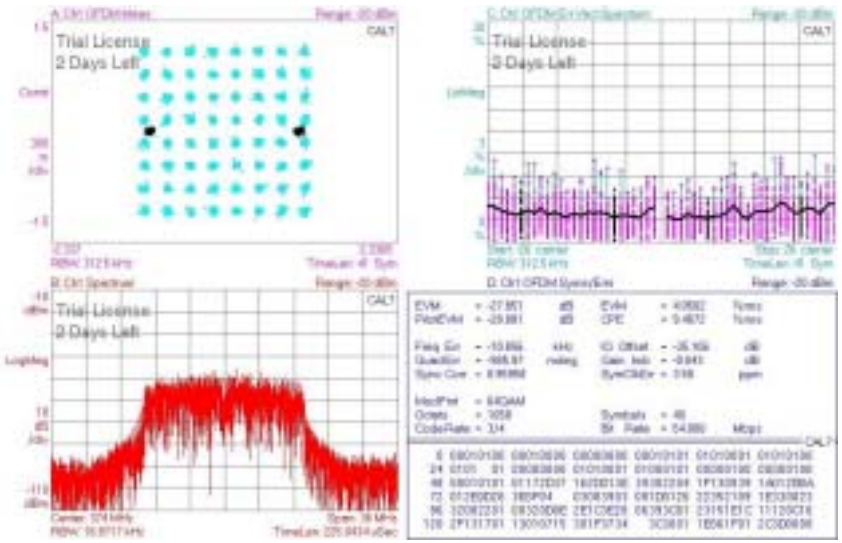
2.4 GHz 64QAM 54 Mbps：

EVM=6.2 % **(-60dBm received power)**



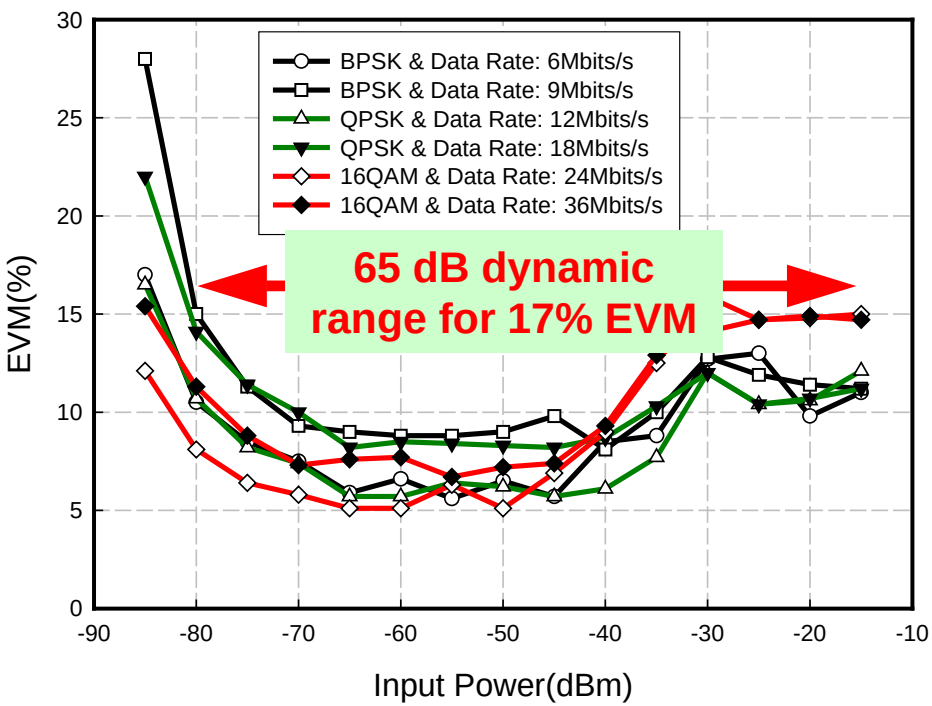
5.2 GHz 64QAM 54 Mbps:

EVM=4.05 % (-60dBm received power)

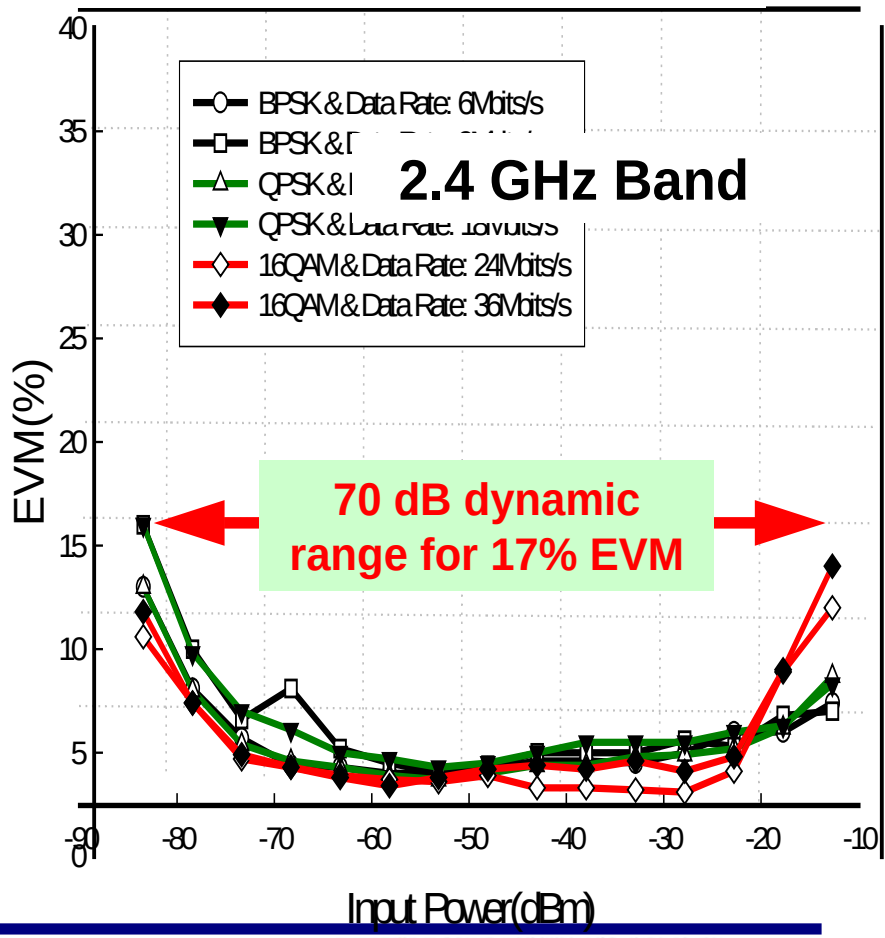


RX(with IF IQ modem) Dynamic Range Test

5.2 GHz Band



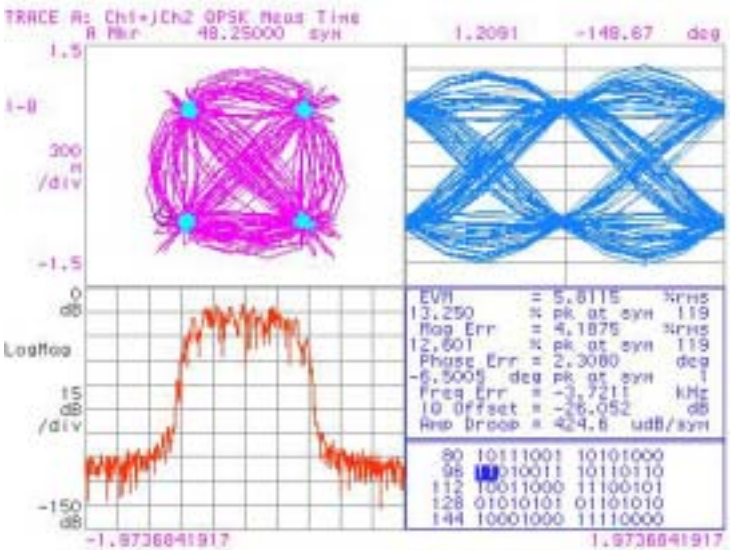
2.4 GHz Band



(II) 2.4/5.2-GHz RF transmitter test

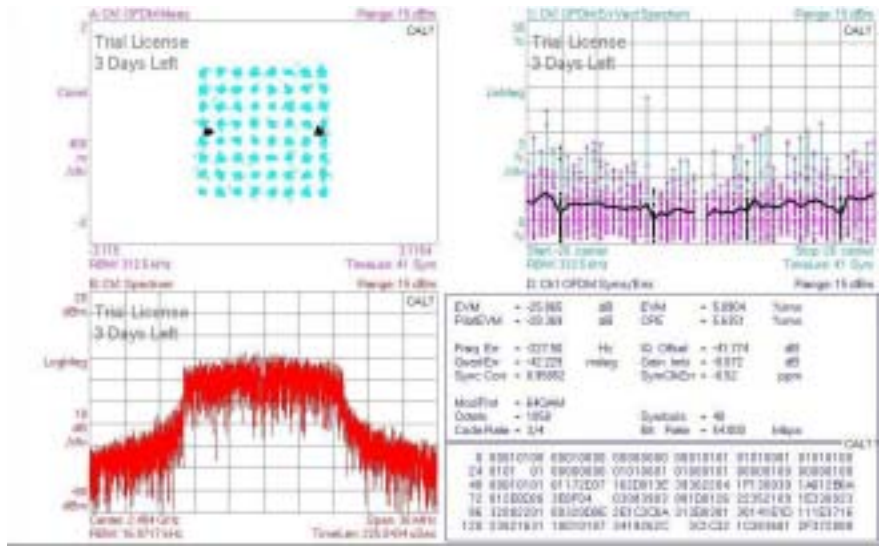
2.4 GHz 12 Mbps QPSK:

EVM=5.8%=-24.7 dB



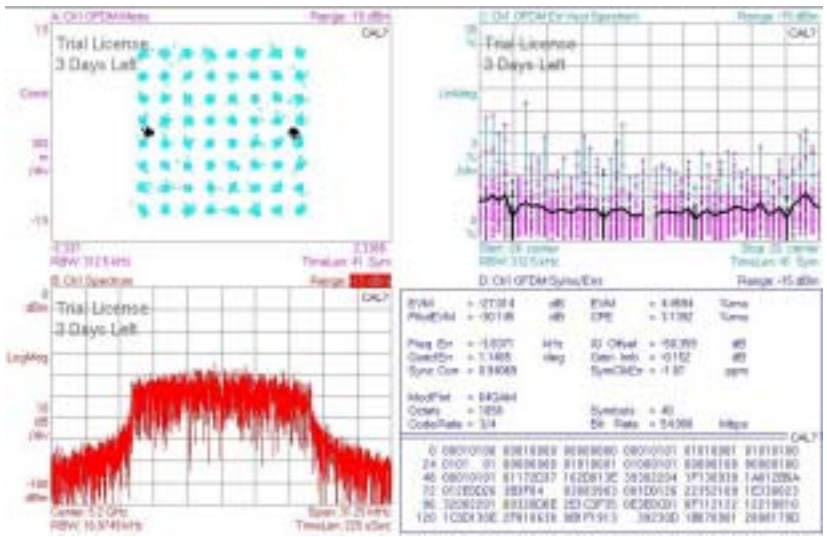
2.4 GHz 54 Mbps 64QAM:

EVM=5.1%=-25.9 dB



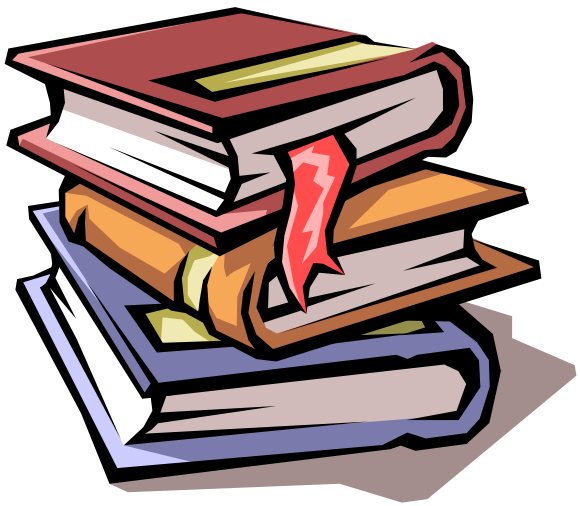
5.2 GHz 64QAM 54 Mbps:

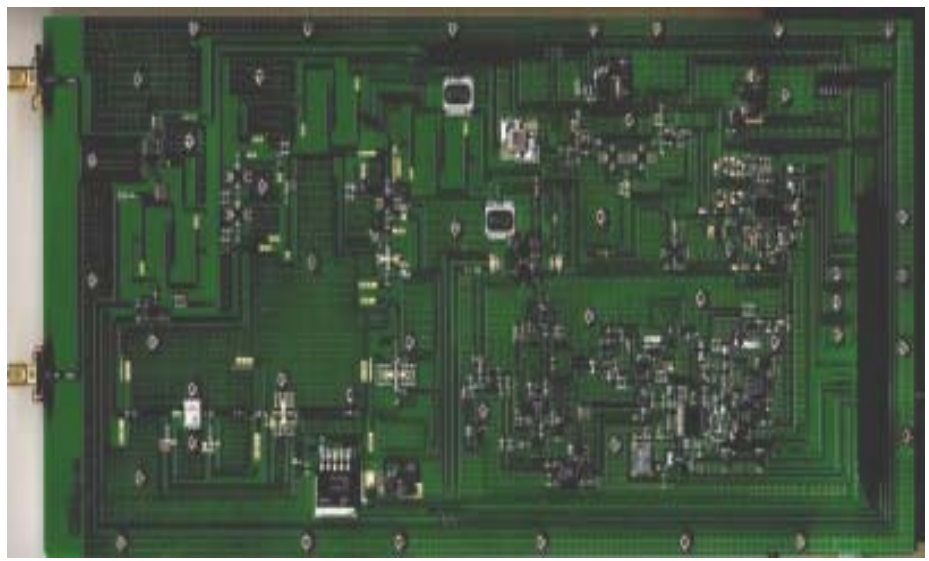
EVM=4.46 %=-27.0 dB



IV. Conclusion

Transform of a *written document* into a physical module





- Examine 802.11a/b/g RF specifications
- Determine RF transceiver architecture
- Calculate and simulate RF transceiver link budget
- Design RF key circuits-MMIC, HMIC
- RF Module Integration and measurement

Thank you

Sincerely appreciate ISSC for partial funding support