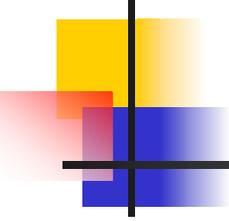


The Fairness MAC Protocol for a Slotted Packet-Switched WDM Ring Network

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Date: 2004/03/08

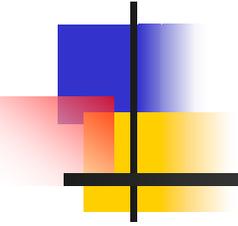
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Outline

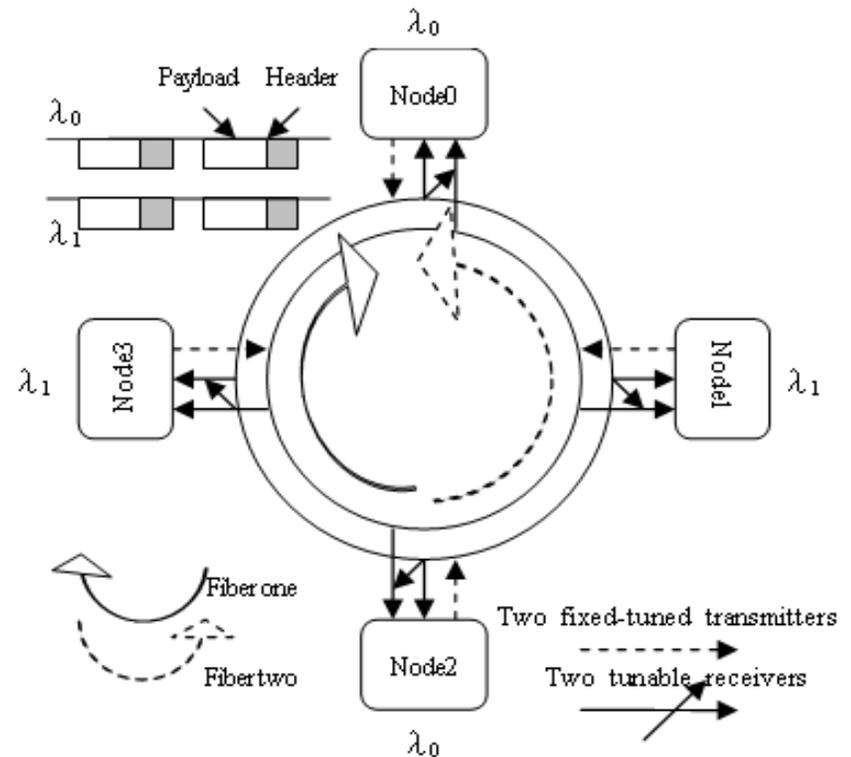
- Network Architecture and Features
- Fairness Problems
- Proposed Multi-FECCA Fairness MAC Protocol
- Simulation Results
- Conclusions and Future Works

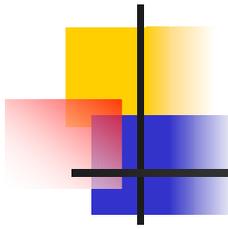
Network Architecture and Features



Full-duplex WDM Slotted Ring

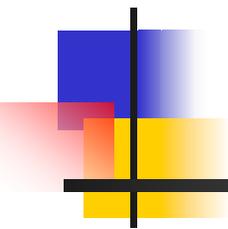
- A full-duplex WDM slotted ring
 - With dual-fiber and a limited number of wavelengths
 - The number of nodes is larger than the number of wavelengths
 - Several slots on each wavelength rotating around the ring
 - All time slots are completely synchronized
- Each node equipped one Fixed-tuned Transmitter (FT) and one Tunable Receiver (TR) in both rings
 - Each node is allowed to transmit only on assignment wavelength and receive on any wavelengths
 - Called FT-TR system



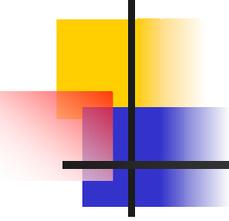


How to Access Ring?

- Wait for an idle slot to fill the payload with its message and then marks the header as busy
- If arrival slot is busy, transmission is simply delay
- Destination removal and spatial reuse mechanisms are employed
 - Each node moves a data which destined for itself and mark this slot as an idle slot
 - This idle slot can be reused



Fairness Problems

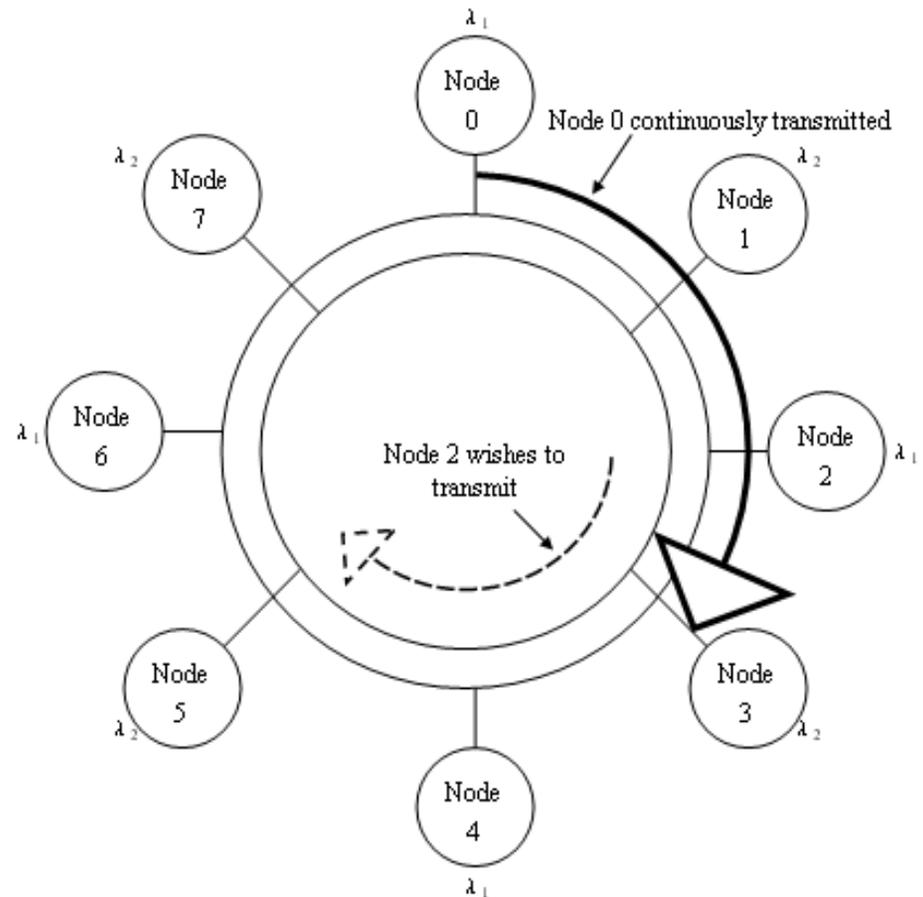


Spatial Reuse

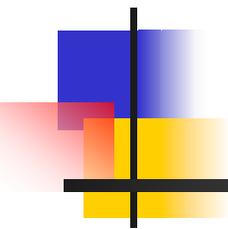
- A spatial reuse mechanism allows each slot can be repeatedly utilized around the ring
 - Can achieve higher network throughput than channel transmission rate
- Lead to fairness problems for each node to access bandwidth

Why “unfairness” occurs?

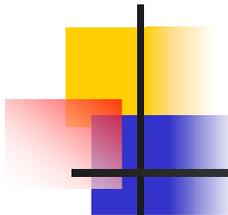
- Fairness problems may occur, especially in un-uniform traffic pattern
 - A heavy traffic node can continuously seize the bandwidth for a long time.
 - Prevents its downstream nodes from accessing the ring
 - The access abilities of those nodes may be influenced
 - “unfairness” occurs



Proposed Fairness MAC Protocol

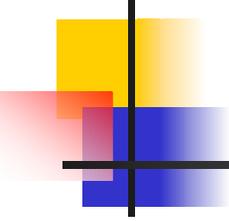


Multi Fair and Efficient Cyclic Control
Algorithm (Multi-FECCA)



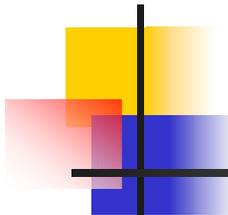
Multi-ATMR Access Algorithm

- The Multi-ATMR control scheme proposed previously is applied on unidirectional TT-FR (Tunable Transmitter - Fix-tuned Receiver) system
- We extend the concepts of Multi-ATMR originally designed for a TT-FR system to a full-duplex FT-TR system.
 - Under full-duplex FT-TR system, Multi-ATMR is independently applies an ATMR mechanism to each wavelength of both rings.



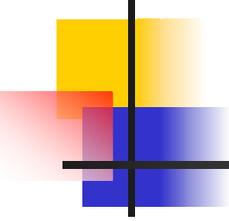
ATMR Control Mechanism¹

- A cycle-based control scheme
 - Each node is allowed to transmit a maximal number of cells within each fairness cycle
 - This maximal number is called *Wins*
 - Each slot composed two segments
 - Payload
 - Header
 - Included a busy address field
 - Each node has two states
 - An active node
 - Has not uses up its transmission quota
 - Has cells stored in the queue
 - An inactive node
 - Used up its transmission quota or has no cells stored in the queue.



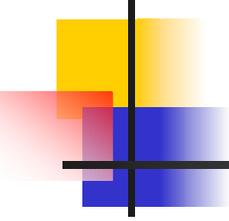
ATMR Control Mechanism²

- Access algorithm
 - Active node
 - Waits for an idle slot to transmit
 - “*Overwrites*” its own address into the busy address field of every incoming slot
 - When a node completely transmit the value of *Wins* cells or has no cells to transmit, it becomes an inactive node
 - inactive node
 - Stops writing its own address in the busy address field
 - When an inactive node finds its own address in the busy address field of an incoming slot, it knows that all nodes have completed their cell transmissions.
 - It then issues a reset signal to start a new fairness cycle.
 - The reset signal circulates around the ring network to notify other nodes that a new fairness cycle is established.



Multi-FECCA Access Algorithm¹

- Notations defined
 - Ring A: the clockwise rotating ring used to transmit data
 - Ring B: the counterclockwise rotating ring used to transmit control message
 - Payload Segment: used to carry a cell
 - Busy address filed: used to record the control messages
 - Active node: defined as in Multi-ATMR
 - Inactive node: defined as in Multi-ATMR

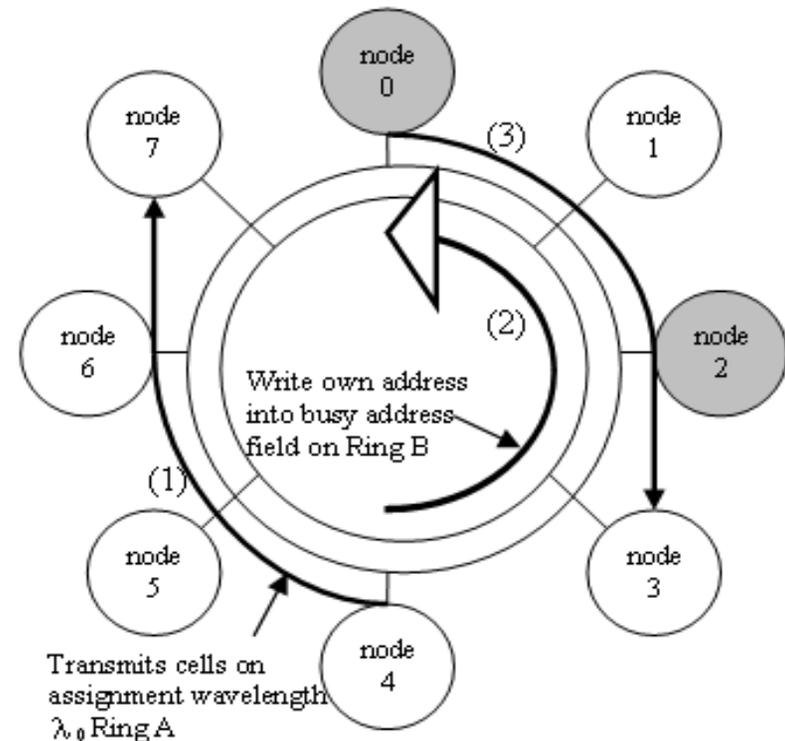


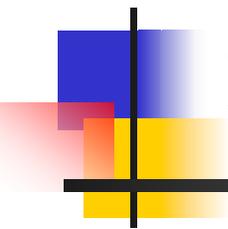
Multi-FECCA Access Algorithm²

- An extension version of Multi-ATMR access algorithm
 - A cycle-based control scheme
 - Used different directions to transmit data and control messages
 - When data are transmitted on Ring A the control messages are transmitted on Ring B
 - A busy address field is included in the header of each time slot
- The Multi-FECCA access algorithm is independently applied to each wavelength of both rings

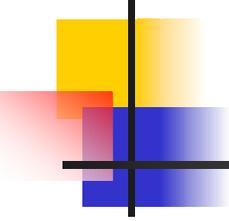
Multi-FECCA Access Algorithm³

- Access algorithm
 - Once a new fairness cycle starts, each active node overwrites its own address into the busy address field of each incoming slot on Ring B
 - By monitoring the busy address field of an incoming slot on Ring B, each upstream node on Ring A can know the current status (i.e., active or inactive) of its nearby downstream nodes.
 - An upstream inactive node on Ring A will know who is its nearest downstream active node
 - An inactive node may be allowed to transmit extra cells on subsequent idle slots without affecting the transmission of its downstream active nodes.



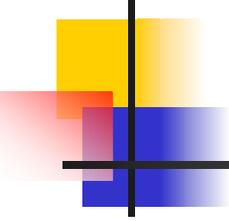


Simulation Results



Simulation Assumptions

- We assume the FT-TR system connects 64 nodes. We also assume that there are 256 slots rotating around each wavelength on the ring with two directional fibers which divided into four different wavelengths $\{ \lambda_0, \lambda_1, \lambda_2, \lambda_3 \}$.
- Under asymmetric load conditions, Nodes 8, 9, 10, 11, 17, 28, 29, 32, 36, 41, 42 and 52 are assumed to be fully loaded. Furthermore, we assume node 9 has 50% of its traffic destined for node 15. All other nodes are lightly loaded based on a Poisson process at a rate 0.05 [cells / slot] with uniform destination distribution.



Simulation Cases

- We present and compare the performance results of the two fairness schemes
 - Multi-ATMR access algorithm: Under this scheme, Each node waits for idle slots to transmit cells and writes its own address into the busy address field of every incoming slot on the assignment wavelength of Ring A.
 - Multi-FECCA access algorithm: In Multi-FECCA control mechanism, each node waits for idle slots to transmit on Ring A and then writes its own address into the busy address field of every incoming slot on the assignment wavelength of Ring B.

Performance of Network throughput

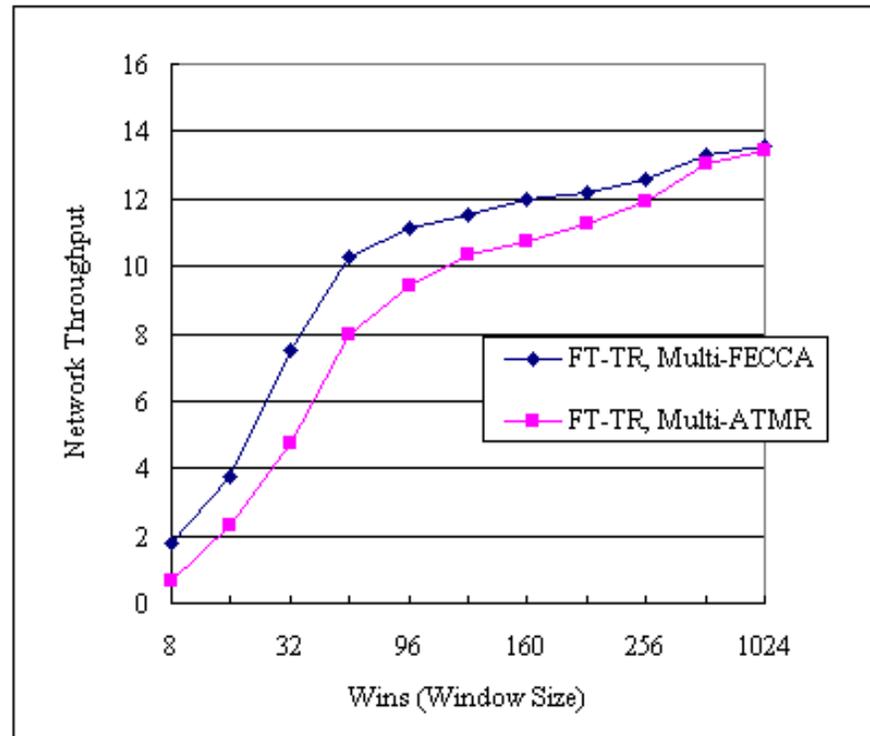
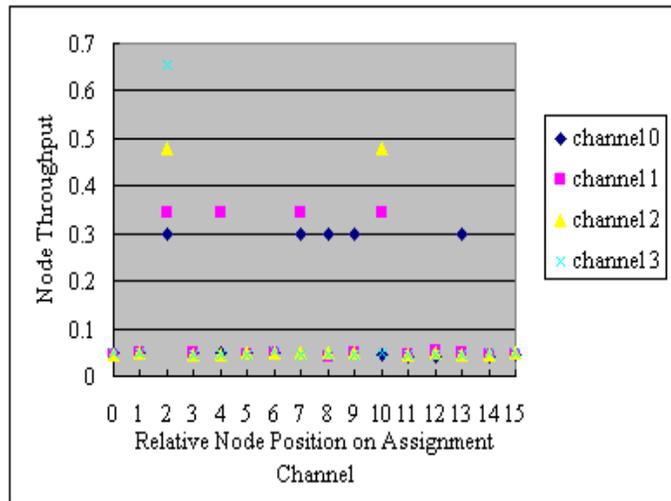
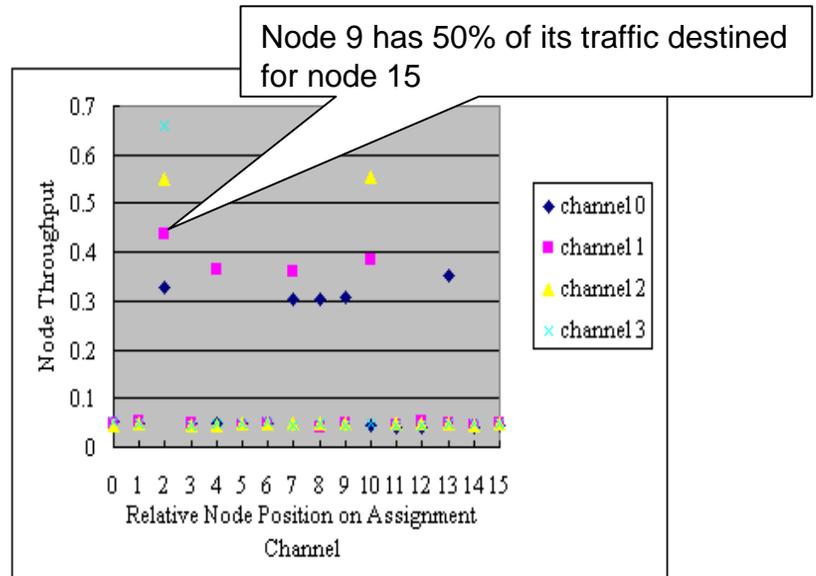


Fig. Network throughput versus *Wins* assignment in full-duplex FT-TR system

Throughput of each Node



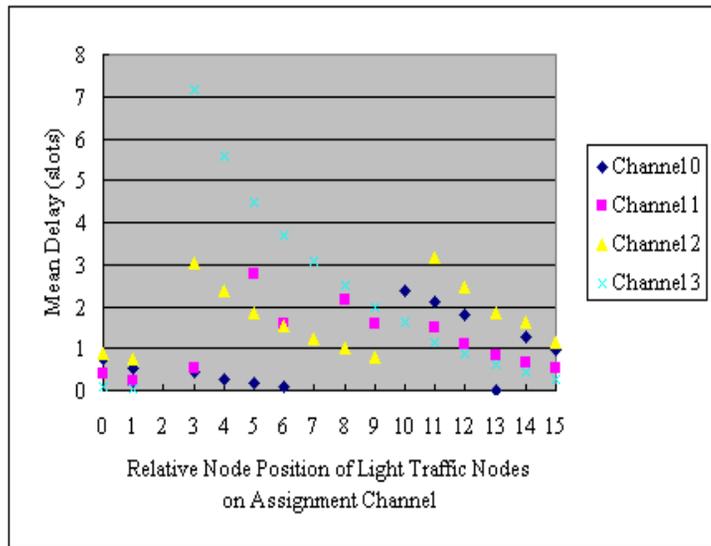
(a)



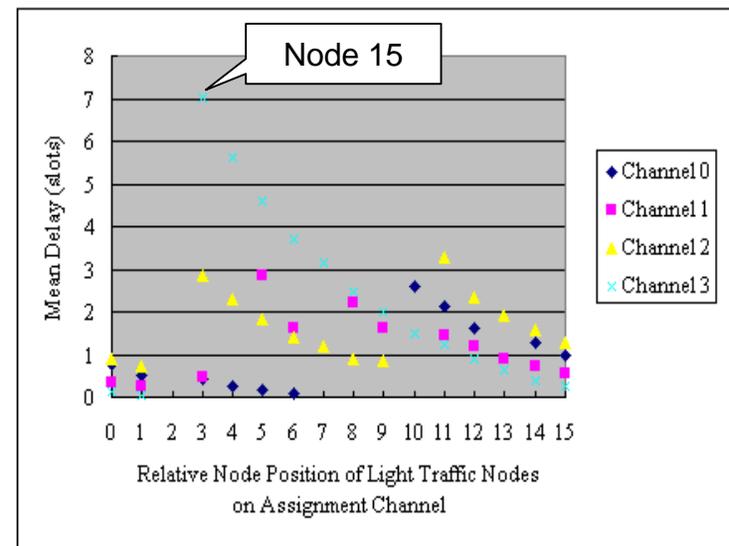
(b)

Fig. Throughput of each node. (a) Multi-ATMR is applied. (b) Multi-FECCA is applied.

Performance of Mean delay

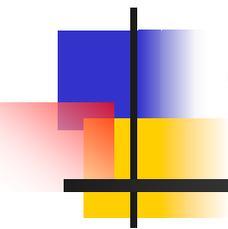


(a)

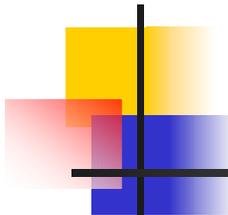


(b)

Fig. Mean delay of light traffic nodes. (a) Multi-ATMR is applied. (b) Multi-FECCA is applied.

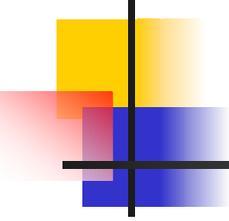


Conclusions and Future Works



Conclusions

- First, extend the concepts of Multi-ATMR control scheme originally designed for a TT-FR system to a full-duplex FT-TR system.
- Then, we proposed the Multi Fair and Efficient Cyclic Control Algorithm, Multi-FECCA.
 - Modified to employ the reverse ring for communication of control singles
 - each upstream inactive node can obtain the information of the on-going activities of its nearest downstream active node
 - may have extra transmission chances without compromising the global fairness
- Performance results shows that
 - Multi-ATMR and Multi-FECCA can successfully operate in a full-duplex FT-TR system
 - Multi-FECCA access algorithm obtains better performance



Future Works

- The use of a tunable receiver has the receiver collision problem
 - One of our future works is to develop an effective strategy for resolving the receiver collision problem
- Another future work is to investigate the Quality of Service (QoS) issue in a FT-TR system



Thanks for your attention